

PowerizeD

Digitalization of Power Electronic Applications within Key Technology Value Chains

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1 Publishable summary

Project acronym	PowerizeD
Project Logo	
Project full title	Digitalisation of Power Electronic Applications within Key Technology Value Chains
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The PowerizeD project aimed to enhance the reliability, lifespan, energy efficiency, and functionality of power devices and systems by integrating intelligent features. This initiative has brought significant societal, economic, and environmental benefits for the European Union (EU). The primary goal of PowerizeD is to reduce power losses and improve the efficiency of power electronics devices and systems across various applications and domains through intelligent control and optimized operational strategies.

To support the overall objectives of the project, **Work Package 2 (WP2)** focused on developing innovative methods, materials, processes, and tools for smart power systems, with a strong emphasis on sustainability. Within WP2, **Subtask WP2.4** concentrates on tools and standards, including the creation of new hardware and software solutions tailored to advanced smart power systems. It also involved the development of novel measurement technologies to evaluate the efficiency of high-performance power electronics arising from the Use Cases (UC). This document provides a summary of the results achieved within the work package. Final results demonstrate significant advancements in the development and validation of DC/DC and AC/DC converters using a Hardware-in-the-Loop (HIL) configuration. The project has successfully implemented a comprehensive automated testing environment for these converters, which enables rapid prototyping and efficient, cost-effective testing. Building on the initial concept and system specifications defined in the first year, the team has developed advanced simulation models, refined testing profiles, and established robust testing procedures. The paragraphs below provide a more detailed description of these deliverables.

The current automated testing system leverages the PLECS RT Box platform, integrating a C-HIL target application model with a script-driven, fully automated, application-specific testing workflow. This approach ensures seamless integration of high-level digital control code and supports model validation through HIL, minimizing manual coding efforts and accelerating development cycles. The report outlines the present status of the automated C-HIL setup, highlights the integration of the Target



Support Package (TSP) with multiple functional blocks for XMC microcontrollers, and details the initial specifications and outcomes of the automated testing process.

An automated toolchain in PLECS was developed for code generation and verification, which now enables the direct integration of high-level digital control code into the testing workflow. The Target Support Package (TSP) has expanded to include 22 functional blocks compatible with XMC1000 and XMC4000 microcontrollers, as well as optimized fixed-point arithmetic tailored for the XMC14xx series. This setup supports comprehensive Hardware-in-the-Loop (HIL) validation, streamlining rapid prototyping and significantly reducing manual coding requirements.

Furthermore, the automated testing system has been enhanced with a SPICE-like solver, facilitating mixed-signal simulations that merge discrete-time control algorithms with highly detailed circuit models. Improvements in numerical methods and netlist parsing have resulted in greater simulation stability and accuracy, reflecting the project's current achievements in automated testing and validation for smart power systems.

The project has achieved significant results in advancing measurement technologies for next-generation power electronics. Comprehensive testing and evaluation have been conducted on the newly developed power electronics solutions, with a focus on key characteristics such as efficiency and their effects on the mains supply. Leveraging the high efficiency and power density achieved through high-frequency switching, the team has introduced innovative measurement approaches. Two distinct prototype setups have been successfully constructed and validated: one employs an electrical measurement method, while the other utilizes a thermal (calorimetric) approach to accurately assess efficiency. In addition, after extensive modeling efforts, a prototype wideband voltage divider has been designed and realized to precisely measure the impact of these advanced power electronics on the mains supply. Reference facilities have been established to ensure accurate and traceable characterization of this voltage divider. These new measurement methods have already been applied to two prototypes from the project's Use Cases, demonstrating their effectiveness. This document outlines the substantial progress achieved in the development and application of advanced measurement technologies for the validation of highly efficient power electronics within the PowerizedD project.

2 Introduction & Scope

The purpose of this deliverable is to present **the summary of final results and progress made in realizing new solutions for hardware (HW) and software (SW) tools for innovative intelligent power systems, as well as measurement technologies to evaluate the efficiency of power electronics solutions created within the project.** This report is intended to serve as a guide for providing definitions for common tools and standards that facilitate the evaluation of the power electronics developed in the various use cases.

2.1 Purpose and target group

This report summarizes the progress achieved in the PowerizeD Innovation Action Project at the work package level (WP2.4). It is intended to suit the reporting requirements set by Chips JU for deliverable reports.

Therefore, the primary target group consists of the Project Officer and Reviewers; the second target group is the consortium itself, seeking to get the complete picture of the project's status. In addition, industry stakeholders interested in innovative power electronics solutions and measurement technologies are also considered target audiences for this deliverable.

The progress and key achievements are summarized as:

- Summary of the status at the work package level.
- Summary of results achieved at the work package level.
- Key achievements during the task / use case / cross-application and domain-level reporting period.
- At the bottom level, work carried out and achieved by the individual partners is presented.

The power electronics solutions developed in the project need significant testing and evaluation on their fundamental properties, such as efficiency and possible impact on the mains. Therefore, new advanced measurement technologies have been developed for evaluating electronic power solutions considering the state-of-the-art properties of power electronics (high efficiency, high power density enabled by high-frequency switching). These new measurement solutions have been applied to evaluate two prototypes developed in the project's Use Cases. As this report is a deliverable, the resource information and financial data have not been presented in this report.

2.2 Contributions of partners

Table 1: Contributions

Chapter	Partner	Contribution
3.1	AIT IFAG PLEXIM PSC SIGN XC	<p><i>Task 2.4.1: HW tools (lead: AIT; participants: IFAG, PLEXIM, PSC, SIGN, XC)</i></p> <p>The HW-Tools task developed a fully automated HIL testing and reporting environment for DC/DC converters using the PLECS RT Box. It includes:</p> <ul style="list-style-type: none"> • A HIL target application model and automated script-based test procedures. • A GUI that abstracts simulation setup, enabling parameter definition without PLECS knowledge. • Automated evaluation of test results (e.g., current ripple within limits) with visual feedback. • Export options for plots, simulation data (Excel), PLECS traces, and full reports tailored to each test type. • Early version were used in the PCIM 2024 paper on multi-level topologies in industrial DC grids.
3.2	PLEXIM	<p><i>Task 2.4.2: SW tools (lead: PLEXIM; participants: AIT, IFAG, SIGN)</i></p>



	<p>IFAG</p> <p>SIGN</p> <p>AIT</p>	<p>PLEXIM</p> <p>Lead developer of the Target Support Package (TSP) for Infineon XMC microcontrollers and the SPICE-like solver in PLECS. Coordinated toolchain development, released public versions, and ensured usability and documentation.</p> <p>IFAG</p> <p>Provided microcontroller resources and toolchain inputs for XMC1000/4000 families. Supported compatibility with DAVE and ModusToolbox environments.</p> <p>Actively tested the TSP to ensure industrial applicability and gave valuable feedback for the SPICE-like solver, improving robustness and industrial relevance</p> <p>SIGN</p> <p>Tested and validated TSP features in use case contexts (UC2.3). Supported application of the SPICE-like solver for converter models relevant to lighting and grid applications.</p> <p>AIT</p> <p>Contributed to testing and verification of the TSP in HIL environments. Collaborated with PLEXIM on Remote Procedure Call (RPC) capabilities.</p>
<p>3.3</p>	<p>VSL</p> <p>PTB</p> <p>UTWENT</p> <p>ZES</p> <p>ZIMMER</p>	<p><u>Task 2.4.3: Measurement equipment and standards (lead: VSL; participants: ZIMMER, PTB, UTWENT, BME)</u></p> <p><u>VSL</u></p> <p>Acquired advanced measurement equipment, including a new Power Analyzer and current sensor from ZES Zimmer, for power efficiency assessments. Power efficiency measurements were demonstrated using the Infineon USB charger and multiple analyzers. VSL also conducted phase characterization up to 5 kHz and assessed the LMG671 analyzer at high voltage and current levels across various power factors. Regular collaborative meetings were held with partners to coordinate activities for Task 2.4.3.</p> <p><u>UTWENT</u></p> <p>Developed and tested an high-accuracy calorimeter for direct measurement of power losses in ultra-efficient converters operating at efficiencies above 98–99%. The current version achieved better than 0.5% measurement accuracy, which is well below the targeted 1%. This evaluation highlighted specific challenges, such as air mixing and the need for improved insulation. Based on these findings, design enhancements have been proposed to enable faster response times and even higher accuracy in future iterations.</p> <p>Switching Loss Characterization: A hybrid SiC/IGBT prototype was constructed, and double-pulse testing (DPT) was performed to accurately assess switching losses under realistic parasitic conditions. These tests have enabled the development of precise loss models using curve-fitting approaches, reflecting actual device behavior in high-performance converter applications.</p> <p>High-Bandwidth Current Sensor: A custom shunt-based current sensor has been developed, targeting a 1 GHz bandwidth, less than 100 pH inductance, and 30 A RMS capability. The sensor incorporates a low-noise, battery-powered amplifier, which</p>



		<p>successfully captures fast switching transients in wide-bandgap (WBG) devices, supporting detailed analysis of high-speed converter operation.</p> <p>Magnetic Component Loss Modeling: core and high-frequency winding losses have been modelled by applying IGSE and HF AC resistance models. These advancements allow for a more comprehensive evaluation of performance trade-offs in magnetic components, contributing to the design of more efficient power converters.</p> <p>Capacitor Loss Characterization: Experimental studies have been conducted to characterize equivalent series resistance (ESR) and capacitance variations with frequency for both electrolytic and film capacitors. The results improve the accuracy of capacitor loss models, particularly under real-world converter operating conditions.</p> <p>ZES Zimmer</p> <p>Developed a precision voltage divider (PVD) demonstrator, featuring a capacitive-resistive helix divider enclosed in a metal housing with protective grounding. This device is capable of operating at approximately 18 kV rms and offers measurement capability from DC up to 150 kHz. The PVD achieved outstanding accuracy, with errors ≤ 333 ppm up to 100 kHz, about 3,000 ppm at 150 kHz, and 0.05% at 50 Hz. Testing confirmed a nearly flat frequency response ($\epsilon \approx 6,000$) and a minimal linearity drift of only 75 ppm across the 1–18 kV range. The measuring amplifier has been developed and finalized, achieving 100 ppm error and less than 60 ns phase delay, showing excellent correlation with simulation data. The demonstrator successfully passed overvoltage endurance testing (26 kV for more than 4 hours), partial discharge analysis, and fast transient testing (250 V/ns at 25.5 kV peak). Areas identified for further improvement include optimized high-voltage inlet designs, increased creepage distances, and the addition of an extra insulator for the high-voltage electrode. Enhancements to portability are also planned for the final version.</p> <p>PTB</p> <p>Established new measurement references have been established for wideband phase characterization of voltage and current sensors, as well as power analyzers. A dedicated test setup was implemented to assess the applicability of the PTB standard to multi-frequency signals, expanding validation beyond single-tone scenarios. For voltage evaluation, a digital-to-analog converter (DAC) with opto-isolators and two calibrators was used to generate synchronized single-frequency signals, which were then combined to produce a two-frequency voltage signal for testing the superposition principle. For current measurements, two transconductance amplifiers generated separate currents at different frequencies, which were summed and measured using a zero-flux converter and the PTB system, further validating the superposition principle. The detailed data analysis and the development of LabVIEW-based software to quantify the impact of intermodulation on overall measurement uncertainty have been planned.</p>
3.4	SIGNIFY PLEXIM XC TUDE	<p>Task 2.4.4: EMC predictions (Lead: SIGN, participants: PLEXIM, XC, TUDE)</p> <p>This task was focused on development of a methodology to predict EMC performance at early design phase. The motivation here is to support the architectural decisions and design process to enhance the possibility of compliance at the release phase. As per EU regulations, EMC compliance is mandatory for</p>



		<p>product release. The EMC compliant product is unlikely to cause interference to the other product in their use case environment.</p> <p>During course of the project, following results have been achieved:</p> <ul style="list-style-type: none"> • Analysis of use cases where such an approach adds value and validating it in the framework of Regulatory requirements. • A preliminary approach to predict conducted emissions has been defined and verified based on 36W power electronics LED converter. • A preliminary approach to predict emission in the conducted range using an in-house 36W power converter has been extended and validated for 50W power converter. • Approach of conducted emission prediction has been extended to predict radiated emission in frequency range 30MHz- 300MHz for 50W power converter. • Models of measuring equipment like Line Impedance Stabilization Network, CDN-E (coupling- decoupling network) have been developed and integrated in simulation test bench. • Conversion of time domain simulation into sampling requirements accordance with CISPR (Resolution band width) have been developed. • Validation measurements of EMI simulated data have been carried out. • EMC study has been conducted to build knowledge and understand the EMI behavior on a fast-switching GaN-based power converter. • The simulation test bench to predict conducted emission was used to design and optimize EMI filter for 3-stage interleaved 1800W totem-pole PFC circuit studied in UC 2.3.
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2.3 Relation to other activities in the project

The Task 2.4.1 is strongly related to Task 3.2.3 LED driver and LV DC distribution grid led by SIGNIFY. Especially in Subtask 3.2.3.4, the automated testing setup has been used to benchmark different multi-level topologies. Based on the simulation results, the most promising topology (flying capacitor) was selected for the development of the prototype for this UC.

Since Task 2.4.1 and Task 2.4.2 are interconnected, and the software created in Task 2.4.2 is tested using the test environment from Task 2.4.1, the development of the test environment has incorporated considerations from Task 2.4.2.

The software developed in Task 2.4.2 has successfully undergone testing and verification within the Task 2.4.1 test environment. The data for Subtask 2.4.2.1, gathered from UC2.3 and CDT4.1, played a crucial role in shaping the initial Target Support Package (TSP) to meet the needs of these applications. Following the preparation of a pre-release version, Signify and AIT conducted a thorough assessment and validation of the TSP. Their feedback has been carefully analyzed and incorporated to enhance its development. As a result, the TSP is now accessible to all PowerizeD members, supporting them in implementing their control algorithms.



Additionally, Subtask 2.4.2.2 received input from CDT4.4, UC1.6a, and UC2.3, which were used to define the requirements and target functionalities of the SPICE-like solver. Although the planned simulations for UC1.6a and UC2.3 could not be completed due to corrupt or incompatible SPICE models, the feedback from these activities was instrumental in refining the solver's capabilities. The solver was successfully tested and verified in UC1.6b (Medium-Power Modular Stationary Charger), where it demonstrated robust numerical performance and accurate modelling. The functionalities required for CDT4.4 have been specified and will be incorporated in future extensions of the solver. Task 2.4.3 primarily related to UCs 1.6c, 2.2, and 2.3, and several on-line and in-person meetings have been held with the leaders of these UCs leaders to assure that the measurement solutions developed in this task met the needs of the UCs. Indeed, the new measurement solutions have been applied to evaluate two prototypes developed in the project's Use Cases. Finally, Task 2.4.3 is linked to Task 2.4.4 (EMC) as both tasks address the emissions (impact on mains) of the newly-developed power electronics solutions within the project.

Task 2.4.4 (CDT4.4 EMC) acts as the source for gathering input in Subtask 2.4.2.2. The main goal was to create a solver that can effectively resolve EMC issues within a system-level simulation while complying with certain limitations that have been set and discussed. The implementation has been tested using UC2.3 as a case study. The simulation test bench of conducted emission was used to design and optimize EMI filter for 3-stage interleaved 1800W totem-pole PFC circuit studied in UC 2.3.

3 WP2.4: Tools & Standards

3.1 Task 2.4.1: HW tools (lead: AIT; participants: IFAG, PLEXIM, PSC, SIGN, XC)

3.1.1 Automated testing and reporting environment

As part of this project, a fully automated testing environment was developed for the validation of DC/DC converters. PLECS is used as a simulation platform and controlled via the XML-RPC interface. The final software includes a functioning HIL target application model and a test procedure that is application-specific and script-based. This setup enables fully automated execution and evaluation of test scenarios, providing a robust foundation for efficient and reproducible verification of unit functionalities.

The automated testing environment includes a graphical user interface (GUI) that offers an abstracted layer to define simulation parameters and selecting the different test cases, without requiring the user to have knowledge of PLECS. This eliminating the need for detailed knowledge of the underlying PLECS simulation model. Figure 1 shows the graphic user interface of the testing and reporting environment after multiple test cases have been simulated. Figure 2 shows the user interface for the simulation test case for the output current ripple test. Within the interface, the maximum allowed ripple for this test case is defined. After the simulation, the interface checks if the ripple is within the limits and shows this in a pop-up window. Figure 2 shows that case when the simulated ripple is higher than the specified limit value. A pop-up window informs the user if the ripple limits were met or not.

The GUI offers the export of plots (of the simulation data), simulation data as excel, PLECS traces and overall report. Depending on the simulation test and topology different plots are exported, as not the whole simulation data is relevant for all simulation.

For example, in the case of the ripple test, only the output current ripple is of interest, so only the output current is plotted. This is shown in Figure 3. Figure 4 shows some example pages of the generated report of the testing environment.

The simulation environment was also used in UC 2.3. LED-Driver and LV DC Distribution Grid. An early version of the testing environment was utilized for the PCIM 2024 publication “Comparison of Multi-level Topologies to Reduce the Components voltage Voltage Stresses when Powered from Industrial DC Grids”.

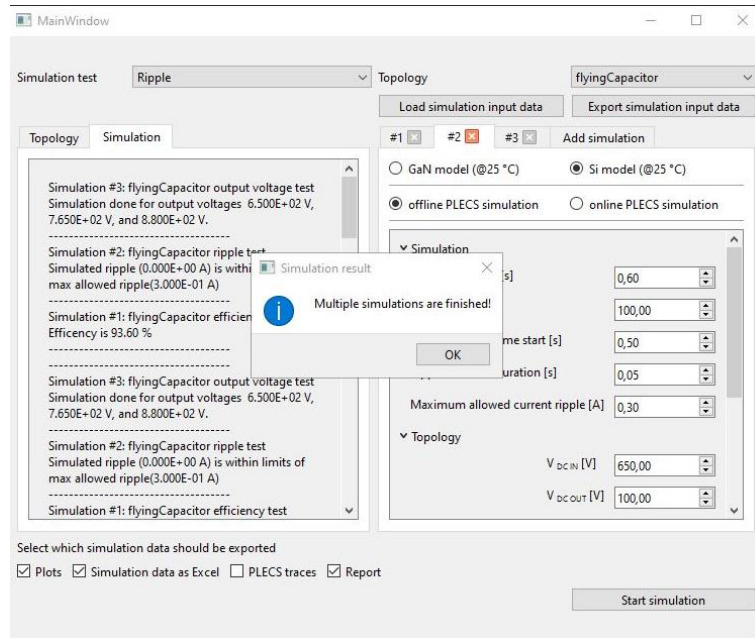


Figure 1: GUI for the automated testing and reporting environment

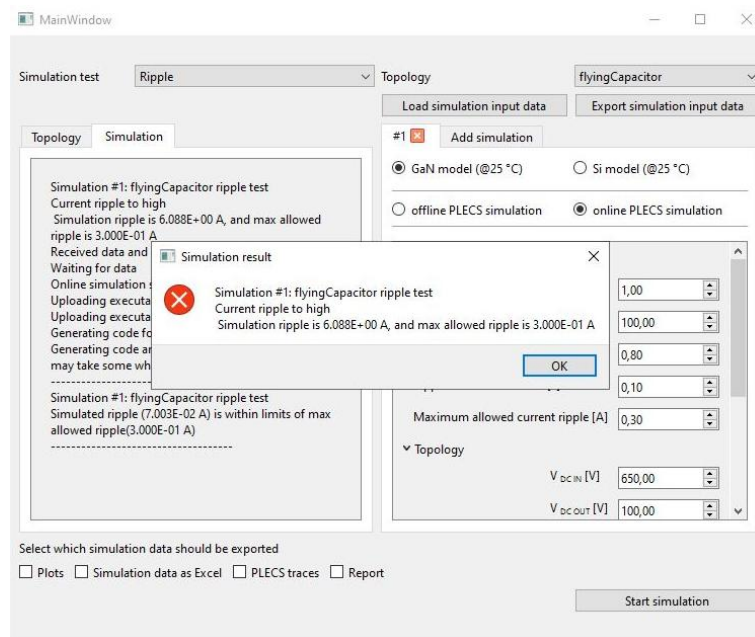


Figure 2: GUI for online simulation of ripple test case, where the simulated ripple was higher than the set allowed maximum ripple

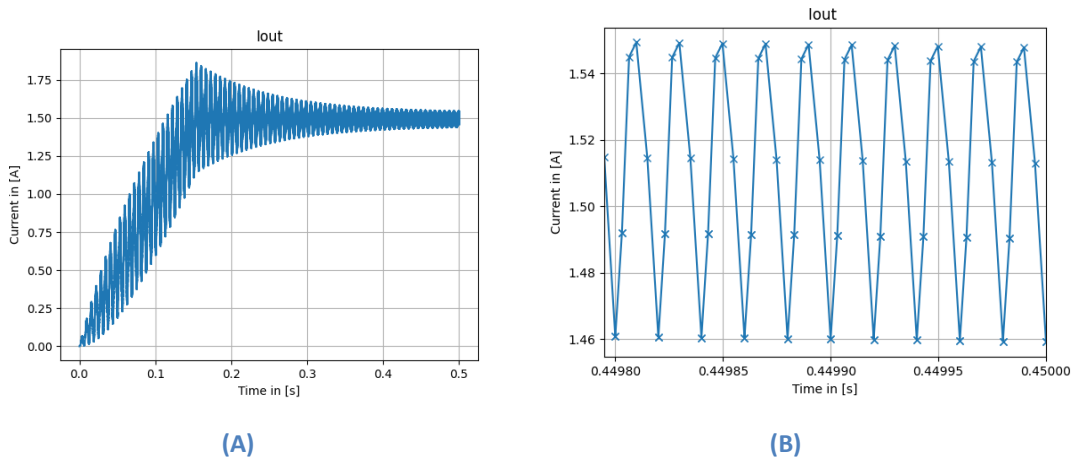


Figure 3: Diagrams generated by the automated testing and reporting environment GUI

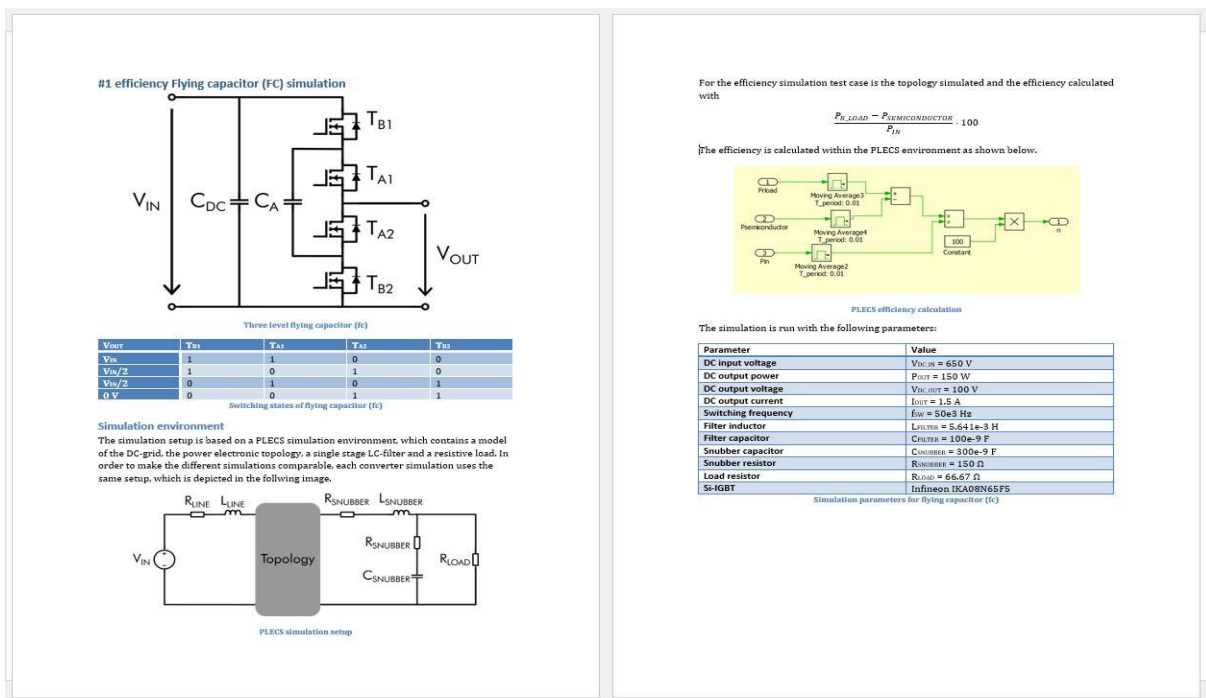


Figure 4: Pages generated by automated testing and reporting environment

3.1.2 Real-time SiC MOSFET model

In the early project stage, Digital Twin developed models for semiconductors showed several small discrepancies, specially in the switching instant, with spice systems. To make a deeper analysis of this issue a small buck converter switched a high speed (1.5 MHz) was created. This board has been manufactured and used to identify and correct most of the discrepancies; among them the merit factors are:

- Correct determination of the parasitic capacitances across MOSFET terminals

- Detecting the switching condition for changing the conduction zone of the MOSFET
- Making a soft-change in the equations of the MOSFET when conduction zone is changed

Figure below provides an overview of the testing scenario with this buck converter board:

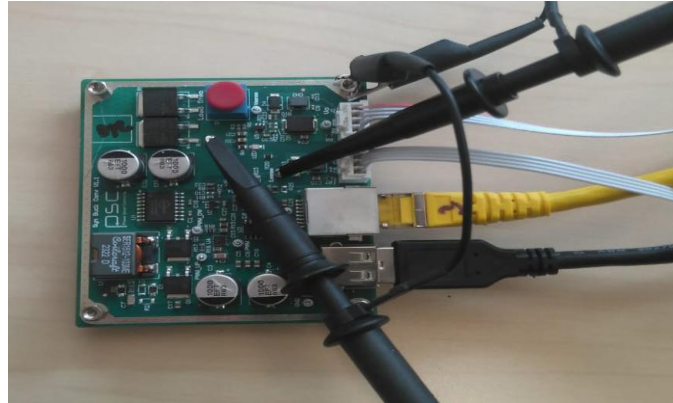


Figure 5: Buck converter test board

The aim of this board is to check the SiC MOSFET model at high frequencies, paying special attention into transition instants. The board greatly helped to improve the performance of the models. In addition, it allowed to discover that there was also another factor that needs correction, that factor is a small deviation among the model and reality as power is being increased. To check it deeper, a double pulse system has been used.

To do this test it is being used the power board shown in picture below. This board allows to increase the power levels to 50 kW at a maximum DC voltage of 800 V. This test, in combination with the conclusions extracted from the small buck board, has provided really helpful feedback to improve and trim the small deviations found in the models. These deviations generate errors below 8%.



Figure 6: Double pulse test board

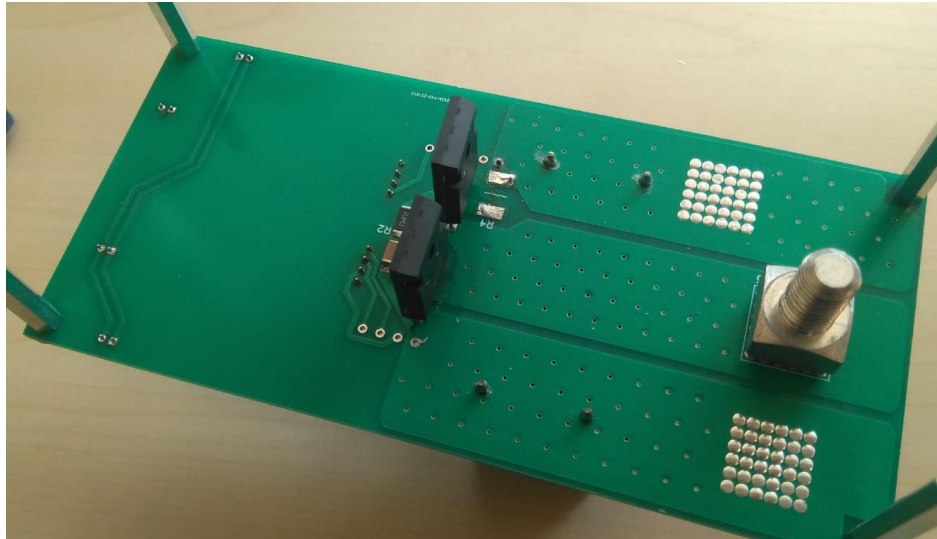


Figure 7: Double pulse test board

In the next picture, of the double pulse test oscilloscope captures is shown. It provides from top to bottom: gating signal, collector voltage, collector current and power losses.

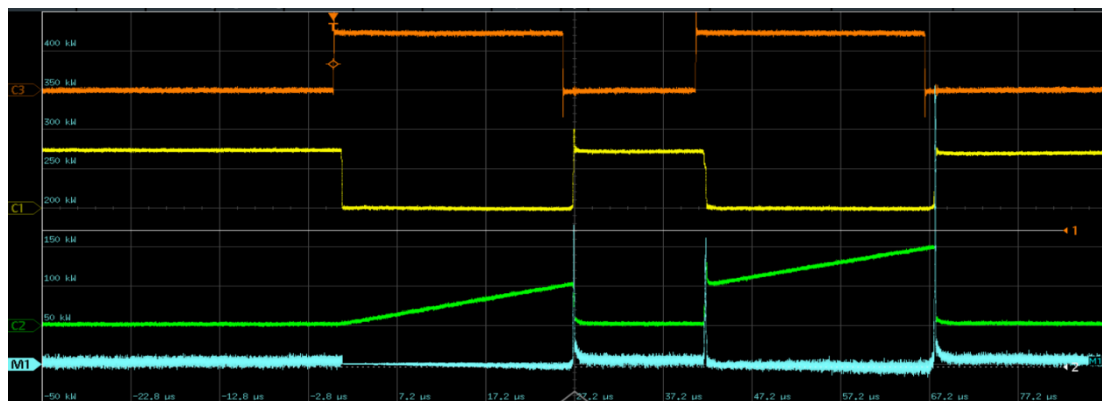


Figure 8 : Double pulse waveforms

Next figure provides a zoom view over the turn-on instant, this was one of the zones where deviation from the model occurs.

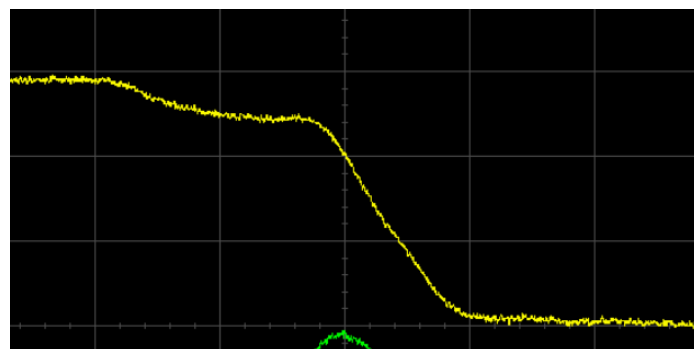


Figure 9 : Double pulse waveforms. Detail of Vce in turn-on instant

By having all this feedback from reality, it has been embedded into the model by generating small modifications of the model parameters. By doing this, the deviation has been reduced.



3.2 Task 2.4.2: SW tools (lead: PLEXIM; participants: AIT, IFAG, SIGN)

3.2.1 Subtask 2.4.2.1 — Target Support Package (TSP) for Infineon XMC

PLEXIM, in close collaboration with Infineon (IFAG), AIT, and SIGNIFY, developed the Target Support Package (TSP) for Infineon's XMC microcontroller family as a cornerstone of the PowerizeD software toolchain.

The TSP establishes a seamless workflow from high-level model-based control design in PLECS to automatic embedded code generation, enabling engineers to implement digital control systems for power electronics applications rapidly and reliably.

During the reporting period, the TSP was expanded to support both XMC1000 and XMC4000 device families, introducing 22 target blocks covering essential peripherals such as ADCs, PWMs, capture units, and protection interfaces. New functionality has been added for runtime-configurable PWM operation, programmable gain amplifiers, and quadrature encoder inputs, allowing broader use in industrial and automotive control applications.

A major focus has been on enhancing usability and simulation fidelity. All input verification features now include contextual guidance and direct error highlighting, allowing engineers to validate their configurations before code generation. The accompanying 67-page user manual was comprehensively updated, making the TSP accessible even to users without extensive microcontroller experience.

The TSP supports Infineon's DAVE™ and ModusToolbox™ development environments, ensuring compatibility with standard industrial workflows. Integration with the PLECS Coder provides automated code generation and deployment for the XMC target hardware, achieving a reduction of development and debugging time by more than 50 % compared to conventional manual coding.

The package has been validated by partners within UC2.3 (LED lighting) and CDT4.1 (HW tools) through Hardware-in-the-Loop (HIL) testing. Feedback from AIT and SIGNIFY led to refinements in the graphical user interface and simulation consistency, ensuring robust performance under real-time conditions. Since its public release (v1.3.1), the TSP has been available for download on PLEXIM's website, supporting all PowerizeD partners and the broader user community.

Overall, the TSP represents a tangible step towards digitalized, automated, and reusable design processes in power electronics, fully aligned with PowerizeD's ambition to reduce complexity and accelerate innovation cycles across domains.

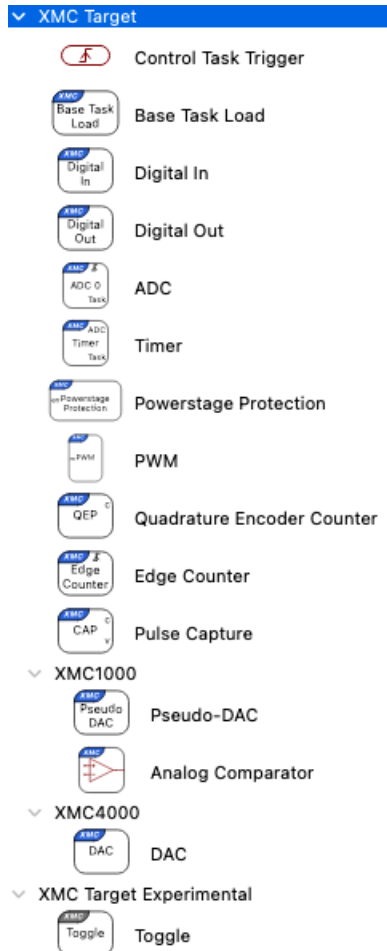


Figure 10: XMC Library in PLECS.

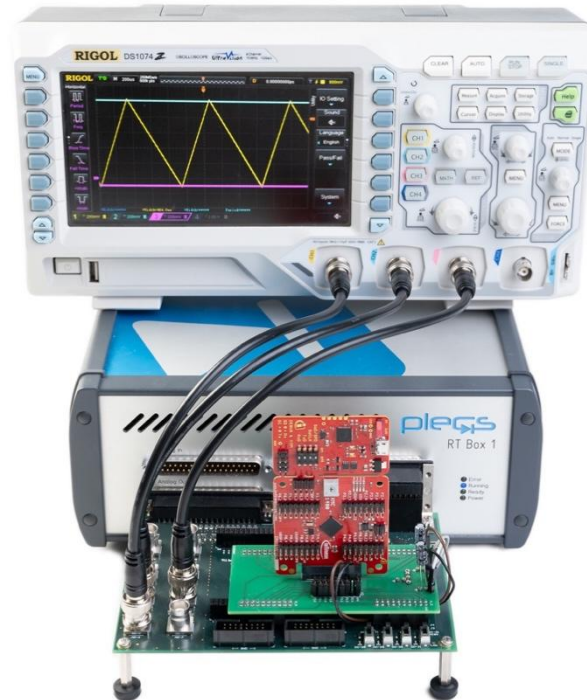


Figure 11: HIL setup for XMC1404.

3.2.2 Subtask 2.4.2.2 — SPICE-like Solver

PLEXIM has developed a SPICE-like circuit solver integrated into the PLECS simulation environment. The solver enables a unified workflow that combines system-level and device-level simulation. This integration allows engineers to assess both idealised and non-ideal component behaviour within a single simulation framework, thereby improving consistency and efficiency in power-electronics design.

The solver features a hybrid numerical engine designed for large and complex converter networks. Numerical performance was enhanced through the adoption of sparse data structures, the integration of the KLU sparse matrix solver, and parallel equation generation. These improvements result in faster computation, reduced memory usage, and higher numerical robustness when analysing switching transients and non-linear circuit behaviour. Convergence stability has been further improved by implementing gmin-stepping and pseudo-transient recovery, ensuring reliable performance across a wide range of operating conditions.

The SPICE netlist parser has been extended to interpret the most widely used SPICE dialects, including NGSPICE, PSpice, LTSpice, and SIMetrix, while maintaining compatibility with standard directives such as .ic, .param, .model, and .subckt. The parser also supports user-defined functions and hierarchical

circuit descriptions, allowing existing SPICE models to be reused directly in PLECS. A dedicated debugging and visualisation interface provides access to solver statistics and model dependencies, facilitating transparent verification of numerical behaviour.

Within PowerizedD, the solver was successfully applied in UC1.6b (Medium-Power Modular Stationary Charger, Figure 14) and UC2.3 (LED Lighting). These applications demonstrated that the mixed-formulation approach shortens model preparation and analysis time while providing accurate insight into the dynamic behaviour of converters under high-frequency switching. The solver proved capable of analysing parasitic effects with a level of detail previously unavailable in system-level simulations.

The developed SPICE-like solver represents a significant step forward in bridging system-level and device-level simulation. It delivers improved accuracy, numerical robustness, and usability, enabling efficient and reliable analysis of modern power-electronic systems within a single consistent design environment.

The technology will soon be made commercially available as the PLECS Spice add-on, extending these capabilities to the wider user community.

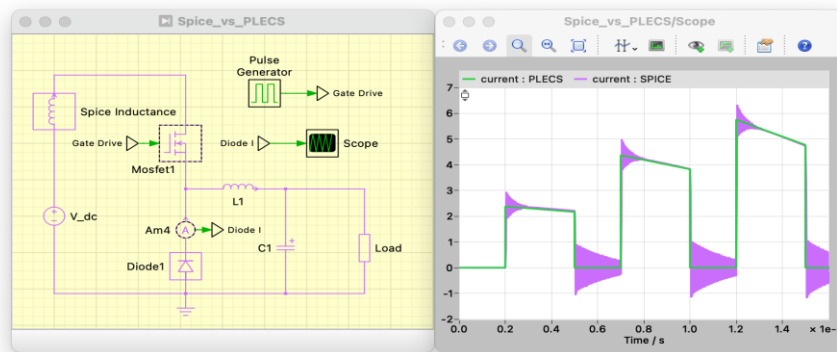


Figure 12: This simulation result depicts two simulations where the MOSFET is either configured as an ideal (PLECS) or non-ideal (SPICE) component.

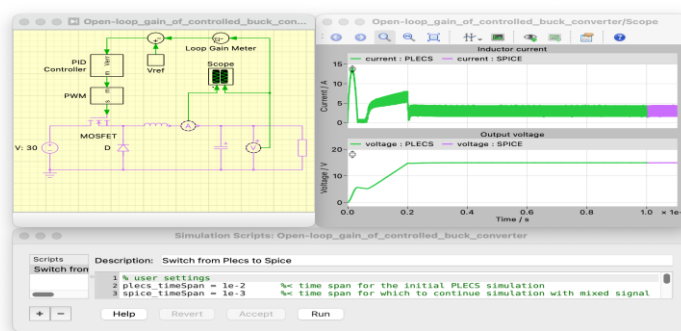


Figure 13: Hybrid simulation; switch from ideal to non-ideal component at key points.

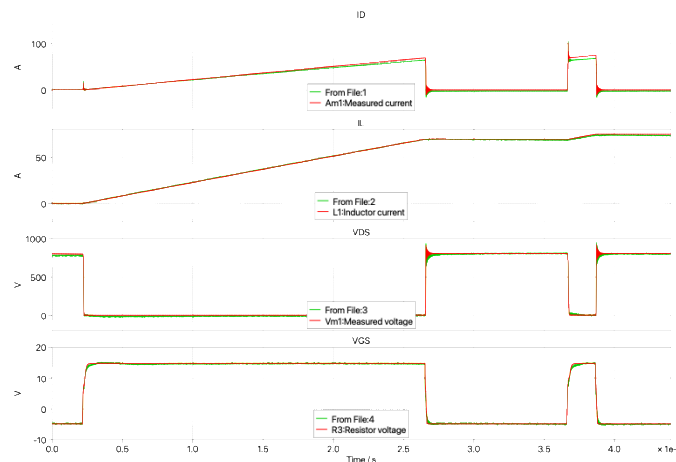


Figure 14: Double pulse test results comparing measured (green, UC1.6b) and simulated (red) waveforms.

3.3 Task 2.4.3: Measurement equipment and standards (lead: VSL; participants: ZIMMER, PTB, UTWENT)

The power electronics solutions developed in the project need significant testing and evaluation on their key properties, such as efficiency and possible impact on the mains. Given the beyond the state-of-the-art properties of the new power electronics (high efficiency, high power density enabled by high frequency switching), new advanced measurement technologies for evaluation of the power electronic solutions on these aspects have been developed. These new measurement solutions have subsequently be applied to the evaluation two prototypes developed in the Use Cases of the project.

3.3.1 Measurement Equipment for overall efficiency.

Power electronics are critical for renewable energy, electric vehicles, data centers, and automation, where efficiency improvements impact overall performance. VSL developed a workflow for high-precision efficiency and power quality measurements by integrating advanced instruments, primary standard calibration, and uncertainty analysis. A ZES ZIMMER LMG671 power analyzer was acquired and characterized along with Danisense PCT200 sensors; DC/AC test plans up to 5 kHz were prepared, a calibration strategy was set to achieve 0.04% accuracy for converters above 98% efficiency, and the power efficiency of Infineon USB charger was measured with WT5000 and LMG 671 power analyzers and an uncertainty budget was prepared. Also a NI PXI 4461 digitizer was characterized for phase accuracy for use in verification of the power analyser.

During the project, VSL surveyed Use Cases 1.6c, 2.2, and 2.3 to confirm the need for more current sensors, leading to the purchase of the PCT200.

Case	Power (kW or kVA) Rated	Input	Input Freq. range (Hz)	Input Current (A)			Input Voltage (V)			Output connection	Output freq. range (Hz)	Output Current (A)			Output Voltage (V)			Expected efficiency (%)
				Rated	Max	Min	Rated	Max	Min			Rated	Max	Min				
1	50	3-ph	50±2	72	86.4	5	400	600	300	DC	DC	83	83	0.5	750	1000	300	99
2	0.1	DC			0.263	0.000758	650	750	600	DC	DC	0.5	0.5	0.03		350	100	95
3	0.6	DC	ripple	1		0	650	715	585	DC	DC+HF ripple	2.1	2.5	0.1	450	520	200	99
4	1.8	2-3-ph	50/60	4.5		0	400	450	350	DC	DC + HF ripple	2.8		0.1	650	715	585	98
5	350	DC	ripple	546			640	920	520	AC 3-ph	up to 1000		850		500			99.5

Figure 15: Specifications gathered from use cases through questionnaire.

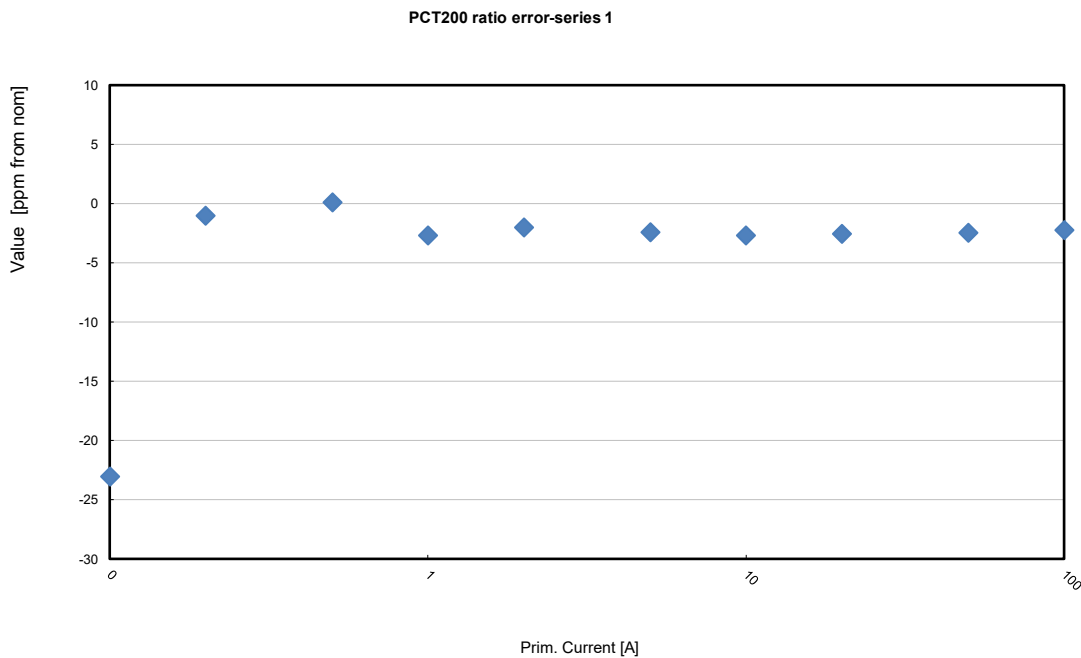


Figure 16: Ratio error analysis of Danisense current sensor PCT-200 across primary current levels.

Characterization of LMG671

The LMG671 has been calibrated at VSL [1] using a high-accuracy power standard. Measurements covered voltages from 10 V to 500 V and currents from 0.02 A to 10 A across various power factors ($\cos \phi = 0, 0.5, 1$) at 50 and 60 Hz. At low power levels, relative uncertainty increases while absolute uncertainty stays almost constant, due to minimum error and noise contributions near the sensitivity threshold. This reduces signal-to-noise ratio and measurement reliability—a factor reflected in the instrument’s uncertainty budget.



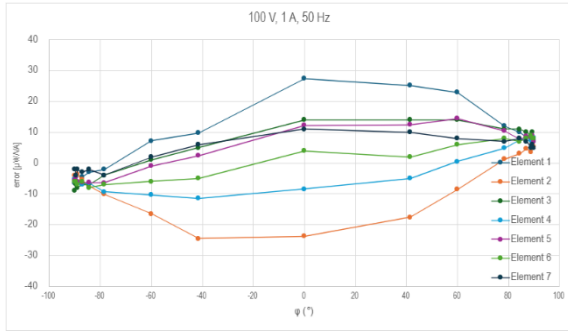
Applied values		Element 1		Element 2		Element 3		Element 4		Element 5		Element 6		Element 7	
Frequency	Voltage	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty
[Hz]	[V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]	[μ V/V]
60	500	-4	17	-44	17	5	17	-29	16	-28	17	-28	16	-32	17
60	200	8	16	-6	16	22	16	-2	16	3	16	-5	16	1	16
60	100	7	17	-13	17	14	17	-3	17	5	16	-10	17	1	16
60	50	-1	17	-14	17	9	17	-7	17	1	17	-9	17	-3	17
60	20	12	17	-12	17	11	17	0	17	2	17	-1	17	-5	17
60	10	45	18	29	18	55	18	41	18	40	18	43	18	37	18
50	500	-10	17	-42	17	4	17	-30	16	-28	17	-28	17	-26	17
50	200	11	17	-5	17	20	17	2	17	9	17	-2	17	3	17
50	100	7	16	-16	17	14	17	-2	16	5	16	-8	17	2	17
50	50	5	16	-16	16	5	16	-4	16	-2	16	-10	16	-10	16
50	20	12	17	-11	17	11	17	-4	17	5	17	3	17	-2	17
50	10	51	18	34	19	60	18	38	18	39	18	40	18	43	18

Figure 17 : Relative deviation and relative uncertainty of all elements of WT5000 at different voltage levels.

Applied values		Element 1		Element 2		Element 3		Element 4		Element 5		Element 6		Element 7	
Frequency	Current	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty	Rel. Deviation	Rel. Uncertainty
[Hz]	[A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]	[μ A/A]
60	10	167	16	239	16	156	16	220.3	16	251	17	164	16	291	17
60	5	41	16	27	16	54	16	21.2	16	35	16	48	16	28	16
60	2.5	5	17	-13	17	-8	16	-4.4	17	-2	17	6	17	-5	18
60	1	12	17	-10	17	-6	17	-6.8	17	8	16	0	17	3	18
60	0.5	23	16	-2	16	14	16	-2	16	11	16	25	16	9	16
60	0.2	13	20	-4	19	-3	18	-20.8	20	12	20	12	20	6	20
60	0.1	20	20	-7	21	-8	20	-18.7	20	9	19	27	19	7	20
60	0.02	-3	42	-32	43	-36	43	-64.3	42	-17	42	-12	43	-10	41
50	10	165	16	233	16	157	16	219.6	16	247	16	161	16	285	16
50	5	42	16	34	16	56	16	27.6	16	38	16	47	16	32	17
50	2.5	7	17	-7	17	-2	17	0.7	17	3	17	12	17	-2	17
50	1	12	17	-16	17	-2	18	-7.4	18	8	17	4	17	4	18
50	0.5	18	16	-2	16	14	16	-10	16	9	16	23	16	7	17
50	0.2	19	17	-7	17	-3	17	-19.7	17	6	17	17	18	7	17
50	0.1	22	20	-4	21	-6	20	-16.4	20	14	21	27	20	8	21
50	0.02	-4	55	-31	55	-39	56	-59.7	56	-16	56	-15	57	-13	55

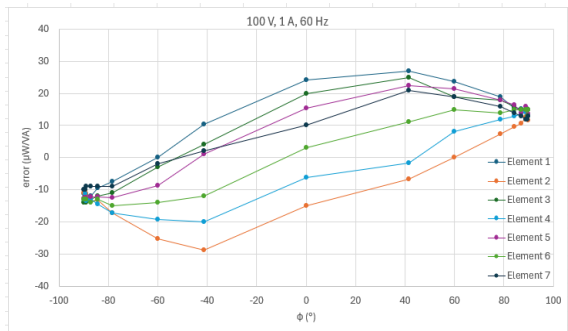
Figure 18 : Relative deviation and relative uncertainty of all elements of WT5000 at different current levels.

At $\cos \phi = 1$, voltage and current are in phase, but residual errors appear due to analyzer offsets and measurement limitations. These systematic uncertainties can be minimized with correction strategies, and further measurements will test error stability and reproducibility.



				PF								
f [Hz]	V [V]	I [A]	cos(φ)	φ [°]	element 1	element 2	element 3	element 4	element 5	element 6	element 7	
					[μWVA]	[μWVA]	[μWVA]	[μWVA]	[μWVA]	[μWVA]	[μWVA]	
50	100	1	0.00 (c)	89.9427	7	5	8	8	7	8	5	
50	100	1	0.01 (c)	89.427	7	6	10	7	9	8	6	
50	100	1	0.02 (c)	88.854	9	4	9	7	8	9	5	
50	100	1	0.05 (c)	87.134	8	5	10	8	9	8	7	
50	100	1	0.10 (c)	84.2608	10	3	11	8	8	7	8	
50	100	1	0.20 (c)	78.463	12	1	11	5	11	8	7	
50	100	1	0.50 (c)	60	23	-9	14	1	14	6	8	
50	100	1	0.75 (c)	41.4096	25	-18	14	-5	12	2	10	
50	100	1	1.00 (-)	0	27	-24	14	-8	12	4	11	
50	100	1	0.75 (l)	-41.41	10	-25	5	-11	2	-5	6	
50	100	1	0.50 (l)	-60	7	-17	1	-10	-1	-6	2	
50	100	1	0.20 (l)	-78.463	-2	-10	-4	-9	-6	-7	-4	
50	100	1	0.10 (l)	-84.261	-3	-8	-7	-7	-6	-8	-2	
50	100	1	0.05 (l)	-87.134	-5	-5	-7	-7	-6	-6	-3	
50	100	1	0.02 (l)	-88.854	-6	-4	-8	-6	-6	-7	-2	
50	100	1	0.01 (l)	-89.427	-5	-4	-7	-4	-5	-6	-4	
50	100	1	0.00 (l)	-89.943	-6	-4	-9	-5	-6	-6	-2	

Figure 19: Error at 50Hz at varying power factors.



				PF								
f [Hz]	V [V]	I [A]	cos(φ)	φ [°]	element 1	element 2	element 3	element 4	element 5	element 6	element 7	
					[μWVA]	[μWVA]	[μWVA]	[μWVA]	[μWVA]	[μWVA]	[μWVA]	
60	100	1	0.00 (c)	89.9427	13	12	15	14	14	15	13	
60	100	1	0.01 (c)	89.427	15	12	15	14	15	13	12	
60	100	1	0.02 (c)	88.854	15	13	15	14	16	15	12	
60	100	1	0.05 (c)	87.134	15	11	15	14	14	15	13	
60	100	1	0.10 (c)	84.2608	15	10	16	13	16	15	14	
60	100	1	0.20 (c)	78.463	19	7	18	12	18	14	16	
60	100	1	0.50 (c)	60	24	0	19	8	21	15	19	
60	100	1	0.75 (c)	41.4096	27	-7	25	-2	23	11	21	
60	100	1	1.00 (-)	0	24	-15	20	-6	15	3	10	
60	100	1	0.75 (l)	-41.41	10	-29	4	-20	1	-12	2	
60	100	1	0.50 (l)	-60	0	-25	-3	-19	-9	-14	-2	
60	100	1	0.20 (l)	-78.463	-8	-17	-11	-17	-13	-15	-9	
60	100	1	0.10 (l)	-84.261	-10	-13	-12	-15	-12	-13	-9	
60	100	1	0.05 (l)	-87.134	-12	-14	-13	-13	-12	-14	-9	
60	100	1	0.02 (l)	-88.854	-12	-11	-14	-14	-13	-13	-9	
60	100	1	0.01 (l)	-89.427	-11	-11	-13	-11	-13	-13	-10	
60	100	1	0.00 (l)	-89.943	-11	-11	-14	-13	-13	-13	-10	

Figure 20: Error at 60Hz at varying power factors.

Power efficiency measurements of the Infineon USB charger

Power efficiency was tested on an Infineon USB charger evaluation board using a Yokogawa WT5000 analyzer at 230 V, 50 Hz and 115 V, 60 Hz, across loads from 28 W to 140 W. Efficiency, calculated as output/input power, matched previous University of Twente results, confirming reproducibility. Next, tests have used a ZES Zimmer analyzer with a detailed uncertainty analysis that accounts for non-sinusoidal input effects.

It was observed that efficiency increases with load due to the reduced impact of fixed losses relative to delivered power. At high output voltage (≥ 20 V), efficiency rises almost linearly with load at both 50 Hz and 60 Hz because the lower output current reduces conduction losses, while switching losses remain moderate. At 50 Hz, efficiency still increases linearly with load at low output voltage (5 V).

At 60 Hz, efficiency drops at higher loads because the charger draws much higher current, thereby increasing conduction and switching losses.

These results highlight the dependence of charger efficiency on both output voltage and input frequency, emphasizing the influence of high currents, DC ripple, and switching timing at low voltages.

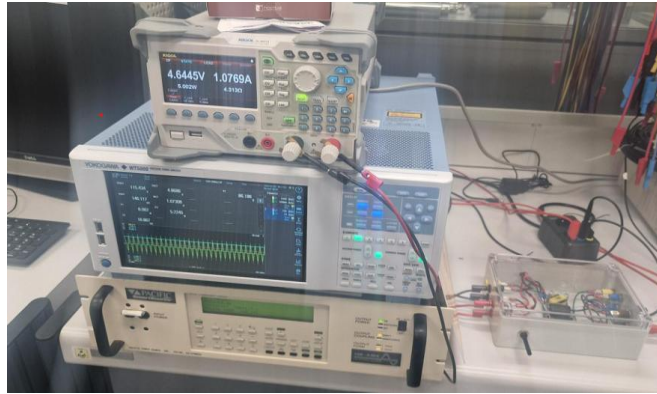


Figure 21: Power efficiency measurement of Infineon USB charger

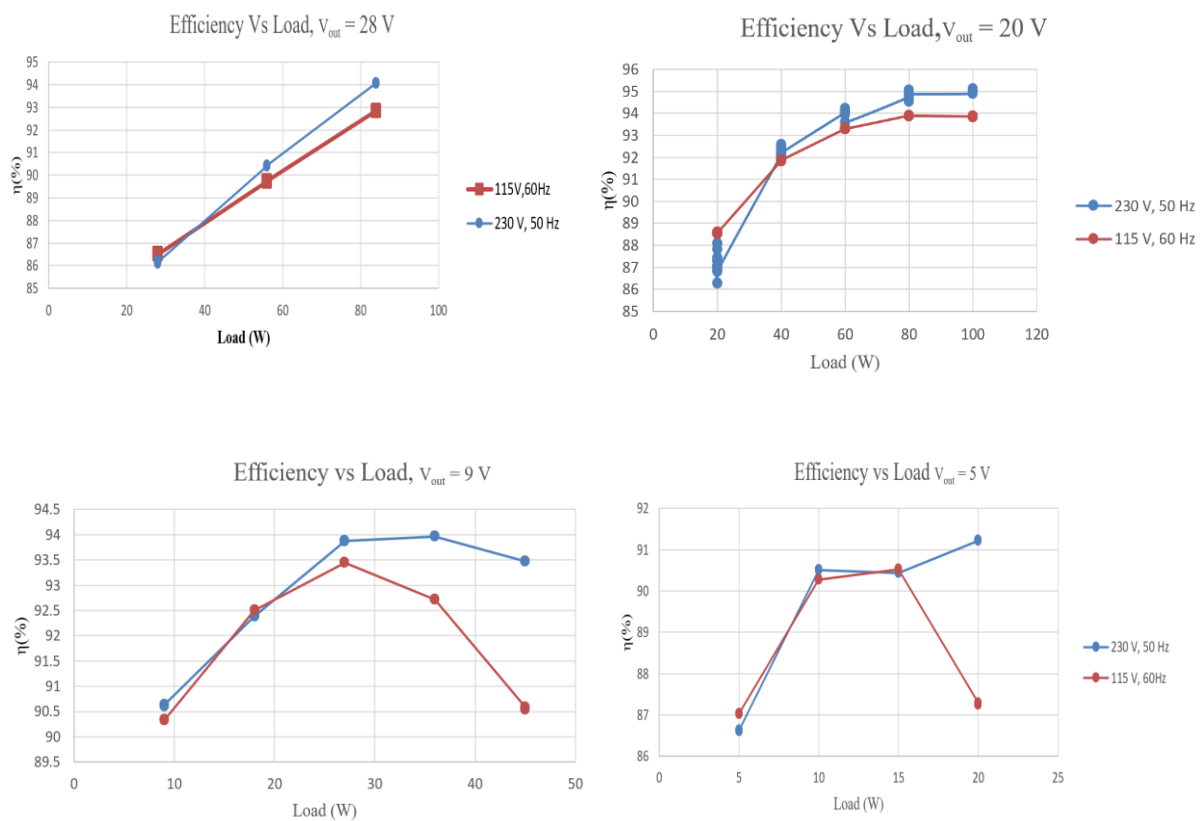


Figure 22 :Efficiency Vs varying Loads at different V_{out}

Phase characterization of NI PXI 4461 2 channel digitizers

The phase response of a system comprising three NI PXI 4461 two-channel digitizers was thoroughly evaluated. A signal ranging from 0.1 to 7 V and spanning frequencies from 50 to 2500 Hz was simultaneously applied to all inputs, and the resulting signals were recorded by the system. Phase differences between channels and modules were subsequently determined based on the acquired data.

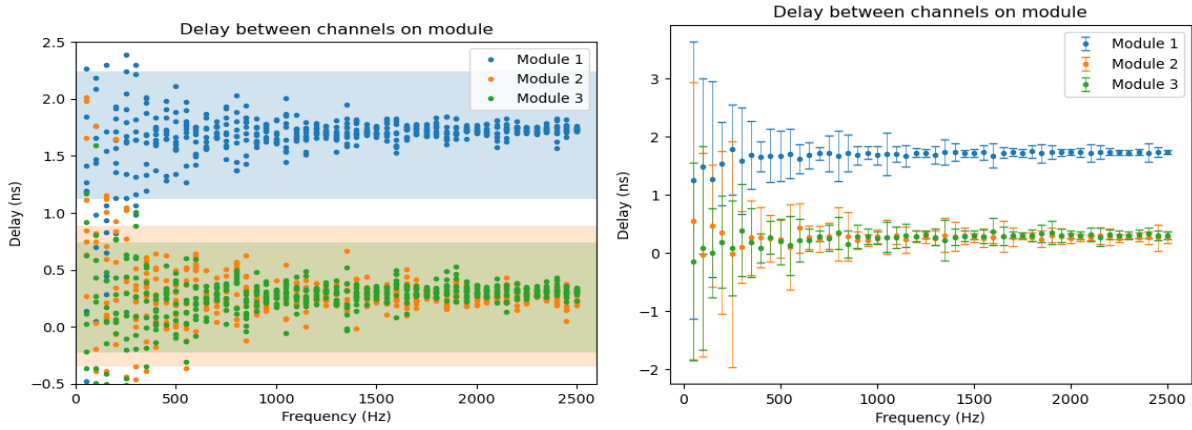


Figure 23. Measured delay between channels on the same module. (a) All samples with uncertainty band and (b) average delay per frequency point with uncertainty. Input signal was a 1Vrms sinewave.

The modules exhibited small, stable between-channel delays of less than 2 ns (Figure 24 (a)). Module 1 showed slightly higher delay than modules 2 and 3. No frequency dependence was detected. These results indicated that all channels in a module shared the same clock, with short or matched lines to the sampling hardware.

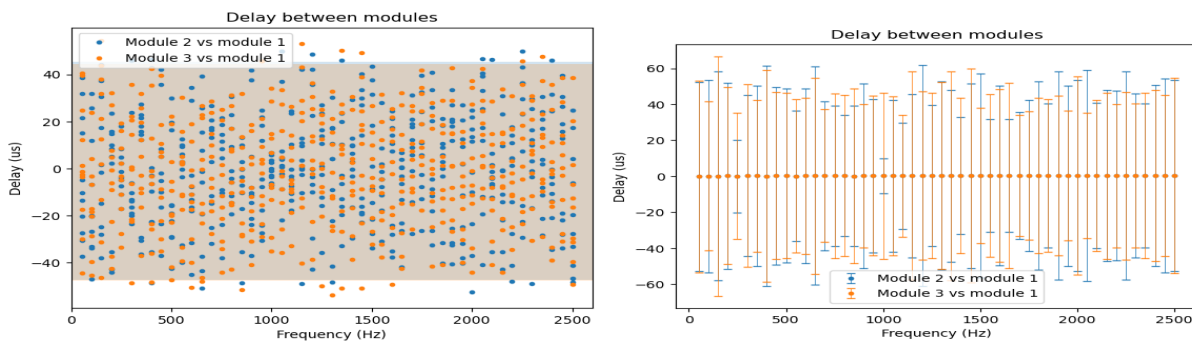


Figure 24. Measured delay between channel 1 of different modules. (a) All samples with uncertainty band and (b) average delay per frequency point with uncertainty. Input signal was a 1 Vrms sinewave.

Delays between modules are around 0.25 μ s (see figure 24 (b)). Results show high uncertainty from sample variance, with no frequency or voltage dependence observed (see table 2), indicating weak synchronization between modules.

Voltage	Module 1	Module 2	Module 3	Module 2 vs 1	Module 3 vs 1
0.1 V	1.74 \pm 0.01 ns	0.26 \pm 0.01 ns	0.30 \pm 0.01 ns	0.29 \pm 3.66 us	0.31 \pm 4.24 us
0.5 V	1.72 \pm 0.01 ns	0.26 \pm 0.02 ns	0.30 \pm 0.01 ns	0.15 \pm 5.48 us	0.06 \pm 6.02 us
1 V	1.73 \pm 0.01 ns	0.27 \pm 0.02 ns	0.30 \pm 0.02 ns	0.25 \pm 5.17 us	0.26 \pm 6.26 us
2 V	1.72 \pm 0.01 ns	0.27 \pm 0.02 ns	0.31 \pm 0.01 ns	0.25 \pm 5.35 us	0.26 \pm 5.97 us
5 V	1.72 \pm 0.01 ns	0.26 \pm 0.02 ns	0.30 \pm 0.01 ns	0.27 \pm 5.32 us	0.27 \pm 6.21 us
7 V	1.72 \pm 0.01 ns	0.25 \pm 0.02 ns	0.30 \pm 0.01 ns	0.25 \pm 5.38 us	0.26 \pm 6.03 us
mean	1.72 \pm 0.01 ns	0.26 \pm 0.02 ns	0.30 \pm 0.01 ns	0.24 \pm 0.04 us	0.24 \pm 0.08 us

Table 2: Delay measurement results for different voltage levels



Earlier measurements confirmed delays of 1.75 ± 0.01 ns, 0.28 ± 0.01 ns, and 0.33 ± 0.01 ns between channels of modules 1, 2, and 3, respectively. However, module-to-module delays varied significantly: -2.77 μ s between modules 1 and 3, and 10 μ s between modules 1 and 2, likely due to incorrect system configuration affecting synchronization.

Next, a voltage divider (1:101 ratio) has been characterized using the calibrated setup. Calibration at 50 Hz for input voltages from 10 V to 460 V used a power analyser as the reference instrument, or alternatively an IVD with calibrated digitizers.

3.3.2 New calorimeter for determination of overall efficiency and losses in high-efficient power electronics.

The University of Twente (UTWENT) developed a calorimeter for measuring extremely low power losses in high-efficiency power electronics. Traditional electrical measurement methods suffer from accuracy problems when efficiencies are in the 98–99% range because they measure the loss indirectly by subtracting output power from input power. A calorimeter overcomes these problems by measuring the loss directly from the heat generated by the DUT.

UTWENT developed a mini calorimeter, which is designed to measure power loss in small devices or inductors up to 50 W. Inside the calorimeter, air is circulated over the DUT and a reference heater. Temperature is measured at a point where the heat from the DUT and the reference heater is properly mixed. This is the control point and is kept at a constant temperature using the reference heater. Once equilibrium is achieved, the DUT is switched on, and the reference heater uses less power to maintain the same temperature at the control point—proportional to the loss in the DUT. The power loss is the difference in power of the reference heater when the control loop is settled.

To make the system more responsive, a water-cooling system is added to the air circulation path. Temperatures are monitored by a multimeter with a scanner card, while the control system and power measurements are managed by a computer.

During development and testing, the initial prototype achieved an accuracy of about 2%, limited by poor thermal mixing. After several modifications, including the addition of an inner compartment for improved heat mixing, the measurement error was reduced to below 0.5% for 10 W losses, meeting and surpassing the 1% target.

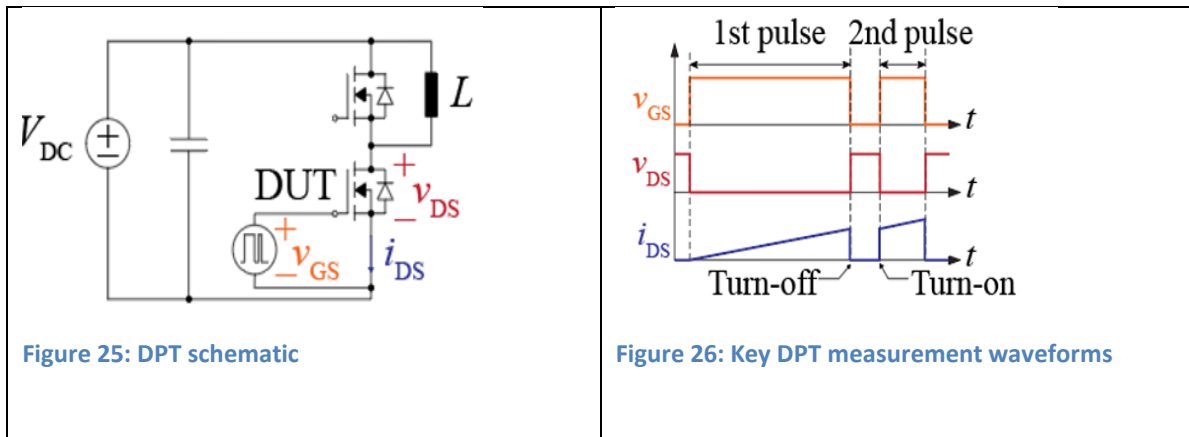
Future improvements aim to enhance usability and speed by reducing insulation thickness to lower thermal resistance and response time, without compromising accuracy due to the robustness of the new measurement approach.

3.3.3 Power loss measurement and modeling of power electronic components

Power electronic components inherently generate losses that affect system efficiency, thermal performance, cost, and reliability. In converters, the primary sources of loss are semiconductors, magnetic components, and capacitors. Their performance—defined by metrics such as power loss, thermal behavior, cost, and lifetime—ultimately shapes the overall converter performance. Among these, power loss is particularly critical. Accurate loss measurement provides insights into the underlying mechanisms, while precise modeling enables designers to evaluate trade-offs early in the design phase. Together, these approaches supported more effective research and optimized power

electronic design. In this project, UTWENT has investigated the suitable power loss characterization methods of the main components.

The power losses of semiconductor devices can be broadly divided into conduction losses and switching losses. With the increasing demand for high-power-density converters, switching frequencies have risen into the hundreds of kilohertz and even the megahertz range, making switching losses the dominant contributor. The adoption of wide-bandgap (WBG) devices, such as silicon carbide (SiC) and gallium nitride (GaN), further complicates loss characterization due to their extremely fast switching transients, with rise and fall times on the order of nanoseconds. A widely used method for switching loss evaluation is the double-pulse test (DPT), as illustrated in Fig. 25 and 26.



In this method, the switching energy is determined by integrating the product of the measured switch voltage and current during the transient,

$$E_{SW} = \int_{t_0}^{t_1} v_{DS} \cdot i_{DS} dt$$

To study this, the UTWENT developed a hybrid two-level converter prototype combining SiC MOSFETs and IGBTs in a parallel configuration, as shown in Fig. 27. The hardware prototype, presented in Fig. 28, uses a phase leg configured as a half-bridge for DPT measurements. For accurate transient measurement, a non-intrusive miniaturized Rogowski coil (CWT3) is employed for current sensing, while a high-bandwidth differential probe (Micsig DP700) is used for voltage measurements.

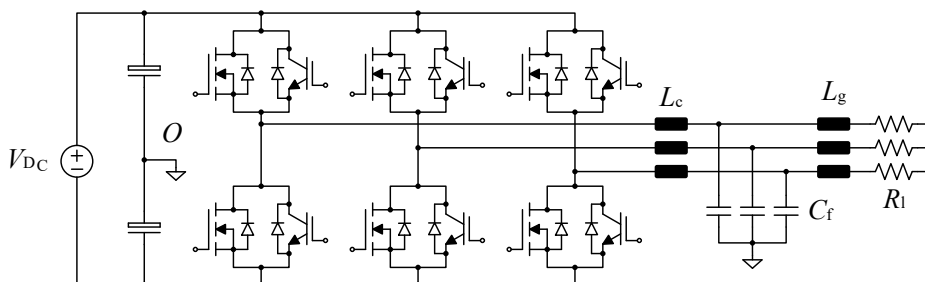


Figure 27: Hybrid converter schematic



Figure 28: Hybrid converter hardware for DPT

The measured switching energies, shown in Fig. 29 & Fig. 30, exhibit a clear dependence on both switched voltage and current, consistent with manufacturer datasheet trends. A key observation is that DPT measurements must be performed on the actual prototype—or an equivalent setup with matching layout and parasitic characteristics—to ensure reliable and representative loss data.

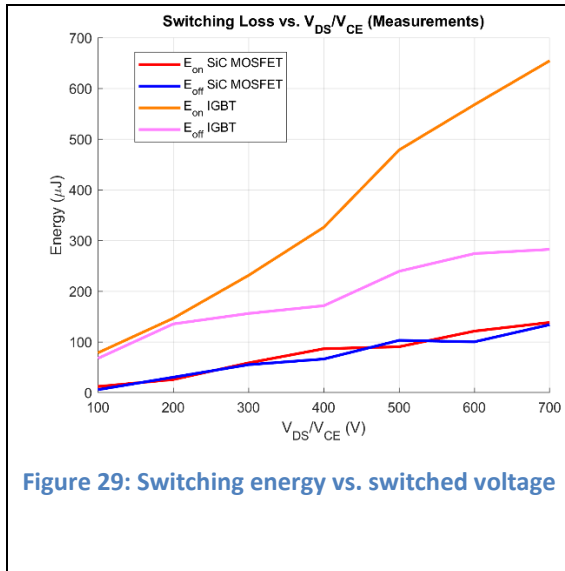


Figure 29: Switching energy vs. switched voltage

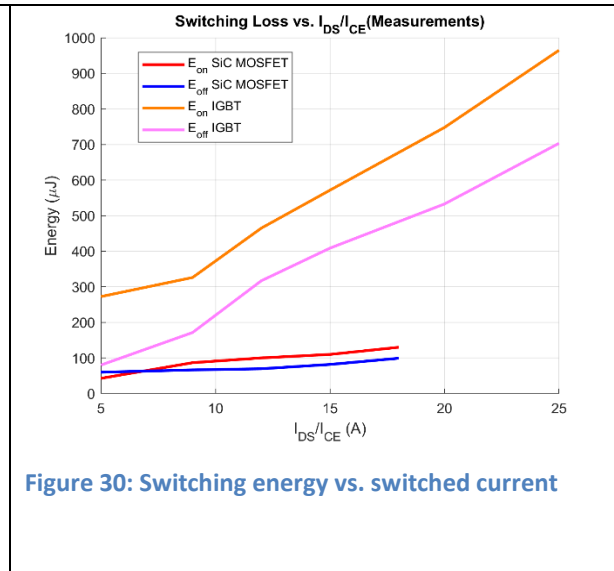


Figure 30: Switching energy vs. switched current

The switching loss can be modeled as a function of the junction temperature T_j , switched voltage V_{sw} , and current I_{sw} . The switching loss of the power semiconductor devices is modelled as

$$P_{sw} = f_{sw} \cdot \left(1 + c_{EGR} \cdot (R_{G,ext} - R_{G,ref})\right) \cdot \left(1 + c_T \cdot (T_j - T_{j,ref})\right) \cdot \left(\frac{V_{sw}}{V_{sw,ref}}\right)^{c_v} \cdot (a_i I_{sw}^2 + b_i I_{sw} + c_i)$$

where c_{EGR} represents the external gate resistance sensitivity coefficient. $R_{G,ext}$ is the actual external gate resistance used in the circuit, while $R_{G,ref}$ is the reference gate resistance in the datasheet during characterization. c_T accounts for the temperature sensitivity coefficient. The exponent c_v captures the switched voltage dependency. $V_{sw,ref}$ is the reference switched voltage from the datasheet. a_i , b_i , and c_i are the curve-fitting coefficients of 2nd order polynomial to describe the dependence of the switching energy on the switched current. The switching energy of the semiconductor devices under operation can be modeled with the data from the DPT with the coefficients obtained by curve fitting. The modeling results can then be added to the design space for further optimization.

Measuring dynamic switching currents in WBG devices is highly challenging due to their extremely fast rise and fall times, which demand current sensors with bandwidths approaching the gigahertz range. Investigations indicate that shunt resistor-based current sensors are suitable for this purpose. However, the off-the-shelf shunt resistor from e.g., T&M research suffers from low actual bandwidth (< 100 MHz) compared to its labeled 2 GHz BW and a high inserted inductance (5-10 nH). These parasitics strongly distort the dynamic behavior of the device under test. To address this limitation, UTWENT has developed a new shunt resistor-based current sensor for measuring the dynamic switching current. The design targeted a 1 GHz bandwidth, an inserted inductance below 100 pH, and a continuous current capability of 30 A RMS. The high bandwidth is achieved using a passive compensation network to cancel the zero introduced by parasitic inductance, while the inserted inductance is minimized through careful control of the current loop geometry. High current handling is enabled by selecting a shunt resistor with very low resistance and adequate power rating. Since the resistance of the shunt resistor is small, the measured voltage across the shunt resistor needs amplification. To pair with the developed current sensor, UTWENT has also designed a low-noise, high BW amplifier circuit. To suppress noise, the amplifier is battery powered. The hardware designs of both the sensor and the amplifier are shown in Fig. 31 and 32. The prototypes will be validated in a GaN-based converter.

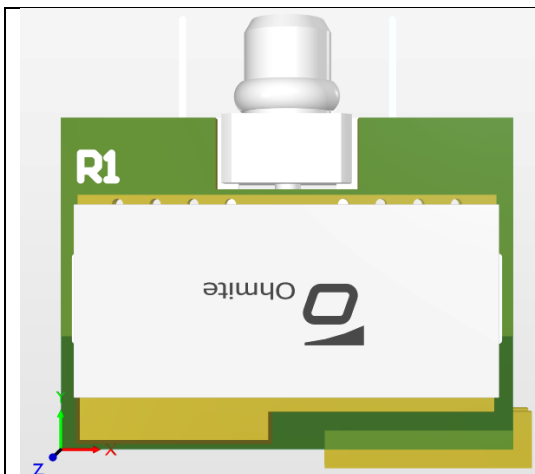


Figure 31: Current shunt sensor design

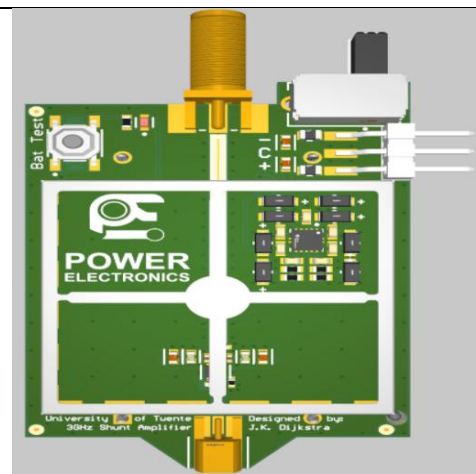


Figure 32: sensor amplification unit.

UTWENT also investigated the loss modeling of the high frequency magnetic components. The modeling of magnetic component losses focused on two dominant mechanisms: core losses and high-frequency (HF) winding losses. Core losses, arising from hysteresis and eddy current effects, are strongly dependent on the magnetic flux density waveform, material properties, and operating frequency. Accurate prediction requires the use of empirical models, such as Steinmetz equation and its improved variants, which account for non-sinusoidal excitations typical in power electronic converters. Here, the Improved Generalized Steinmetz Equation (IGSE) is adopted to evaluate the core losses.

$$P_v = \frac{1}{T_s} \int_0^{T_s} k_i \left| \frac{dB}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha} dt$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos \theta|^\alpha 2^{\beta-\alpha} d\theta}$$

On the other hand, HF winding losses are governed by skin and proximity effects, which significantly increase the effective AC resistance compared to the DC value. It can be evaluated as

$$P_w = R_{DC} I_{DC}^2 + \sum_{n=1}^{\infty} R_{AC}(nf_0) \cdot I_{AC,RMS}^2(nf_0)$$

$$R_{AC} = R_{AC,skin} + R_{AC,prox}$$

The effective AC resistance can be measured with an impedance analyzer. It can also be modeled with analytical models that capture the HF effects on the winding resistance. A comprehensive loss model combining these two aspects has been developed to evaluate efficiency, thermal performance, and design trade-offs of magnetic components in high-frequency power electronic systems.

Finally, UTWENT also investigated the loss modeling and measurement of electrolytic and film capacitors. The total power loss of a capacitor can be represented as the sum of the resistive loss associated with the Equivalent Series Resistance (ESR) and the leakage current loss, with the ESR loss being the dominant contributor. The equivalent circuit model is in Fig.33.

$$P_{loss} = \sum_n R_{esr}(f(n), T) \cdot I_{C,RMS}^2(n) + V_C \cdot I_{lkg}(V_C, T)$$

Datasheets typically provide ESR values at specific frequencies and temperatures, which may not reflect the actual operating conditions in power electronic converters. Therefore, characterizing the capacitor under relevant operating points is essential for accurate loss estimation. A 100-μF electrolytic capacitor used in the DPT prototype is characterized using an impedance analyzer, as shown in Fig. 34. The results show that the ESR and capacitance decreases significantly as the current frequency enters the kilohertz range, and the capacitor losses can then be evaluated using the derived loss model.

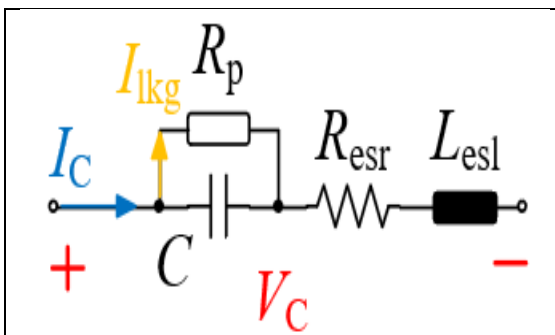


Figure 33 : Equivalent circuit of electrolytic capacitors

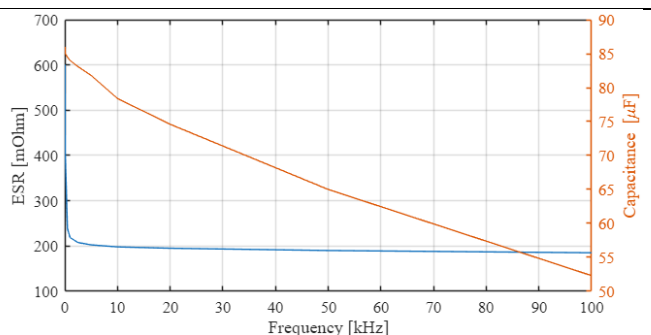


Figure 34 Equivalent circuit of electrolytic capacitors

With this framework, the losses of the main components can be evaluated or measured individually, enabling a detailed breakdown of their contributions.

3.3.4 Development of a new wideband medium voltage divider

ZES ZIMMER (ZIMMER) has successfully completed a new prototype wideband medium voltage divider. One challenge in realizing the latest prototype was that the resistors previously used in the divider cascade were discontinued; a replacement has been found that even has a lower temperature coefficient. Accordingly, the bottom resistors were replaced with ones having the same temperature coefficient.

Another revision of the voltage divider using the aforementioned new resistors was assembled by a skilled technician. During assembly, the work instructions and manufacturability for possible series production were tested. The technician's assessment found no major issues with the current design.

The in-house high-voltage (HV) feedthrough is ready for variant analysis. Corresponding prototypes were manufactured by the metal workshop at Goethe University. Thanks to our own feedthrough design, the housing height of the voltage divider can be reduced to 240 mm. For safety reasons the housing diameter was increased by 10 mm to 315 mm. The self-built feedthrough now makes it possible to route the HV supply line in a fully shielded configuration from the source to the feedthrough. This suppresses parasitic capacitive and inductive influences and greatly improves the repeatability of the measurement system. The photo below shows the new housing of the high-voltage divider with the attached measurement amplifier and the shielded HV supply line.



The frequency response is now more stable against temperature influences due to the new resistors, and is slightly flatter because of the larger housing diameter. After careful adjustment, the following frequency response of the overall system (voltage divider with measurement amplifier) was measured in the new setup.

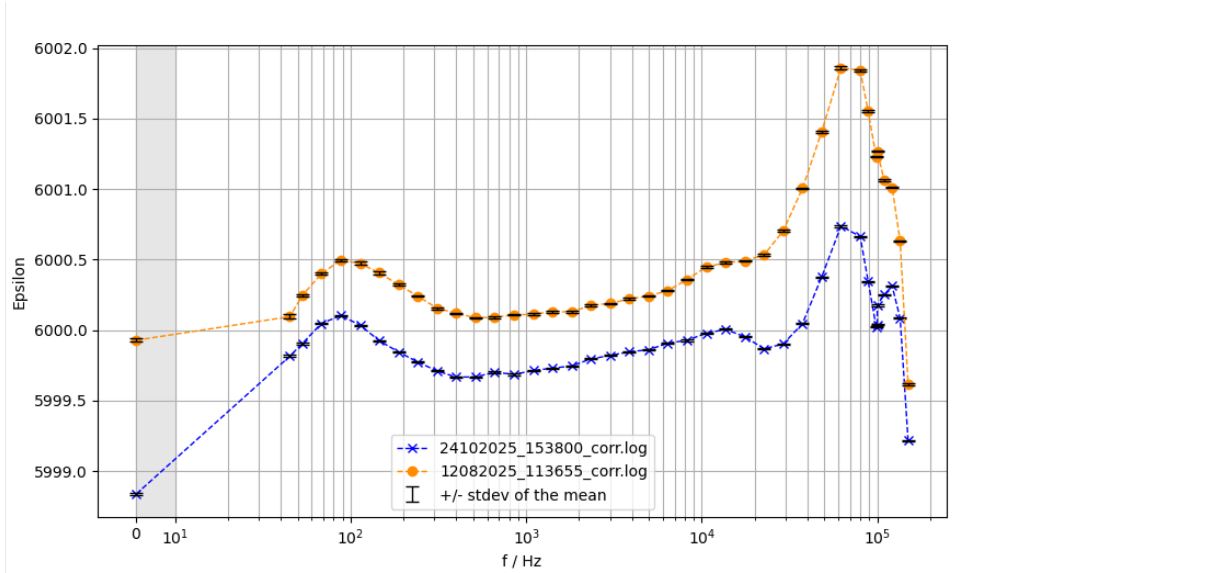


Figure 35 Frequency response of the combined system at a 750 V rms input (HV divider including measurement amplifier). Orange shows the penultimate revision (as in D 2.4.3); blue is the current revision. One division on the x-axis (ϵ) corresponds to 166 ppm. The DC value must be measured separately and is therefore not reliable in this plot.

Many measurements were performed to build confidence in the new setup and to assess repeatability. In particular, the upper frequency range (10 kHz to 150 kHz) is sensitive to the positions of the grounding points. This sensitivity was minimized by using suitable ferrite toroidal cores. For verification, the frequency responses of the HV divider and the measurement amplifier are regularly spot-checked with the newly acquired and calibrated AC standard (a Fluke 5790A).

A test rig to determine the partial-discharge behavior of the self-built HV feedthroughs has been set up as well. Its results are used to select the final design of the HV supply line and feedthrough. Based on that, a final demonstrator of the voltage divider will be built. In addition, a new revision of the measurement amplifier is currently under construction; it includes an additional circuit on the signal output so it can drive long cable runs (on the order of 10 m or more) between the amplifier and the measuring instrument.

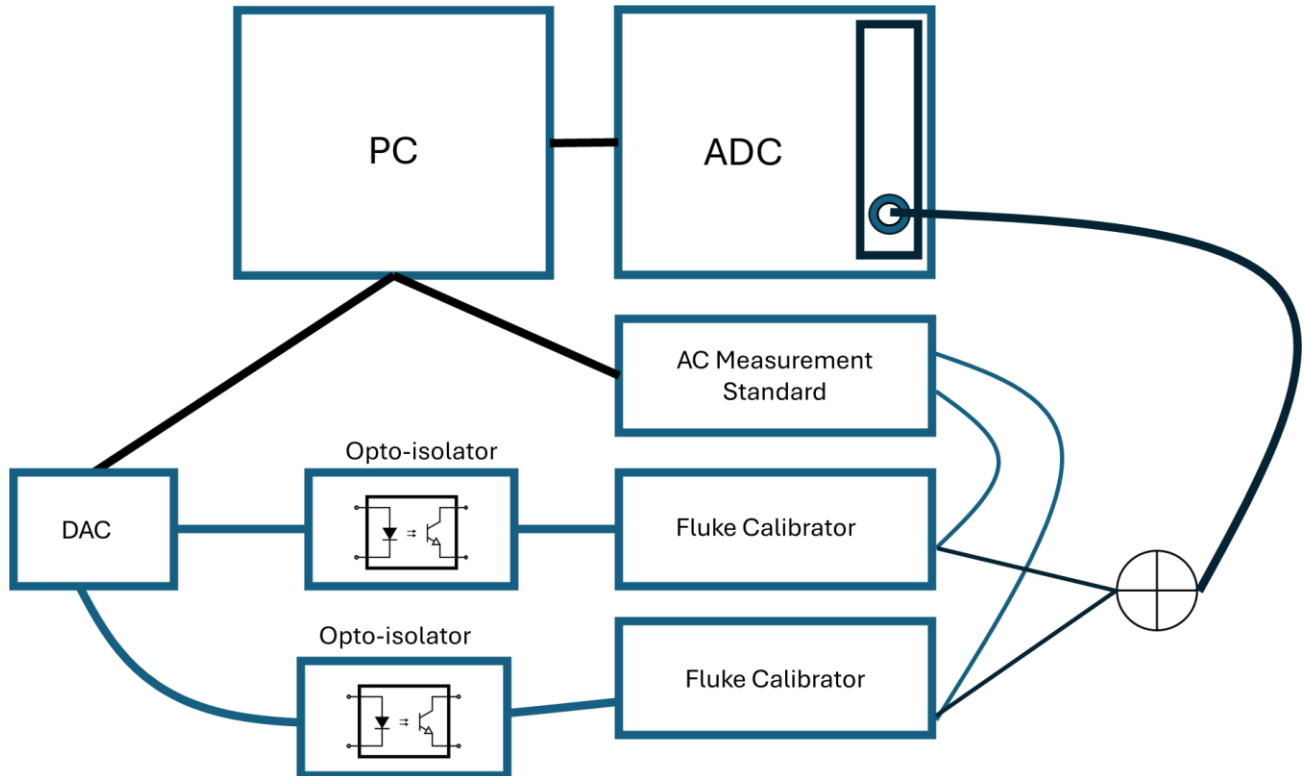
3.3.5 New measurement references for wideband phase characterization of voltage and current sensors and power analyzers

The PTB standard has been validated for single-tone signals, necessitating further investigation to confirm its applicability to multi-frequency signals. To address this, a dedicated measurement setup was implemented to evaluate the linearity of the measurement system. By determining the relevant parameters through direct measurement, the induced nonlinearity and its contribution to the overall measurement uncertainty can be systematically calculated. This approach ensures that the reliability of the system is properly assessed for complex signal conditions.

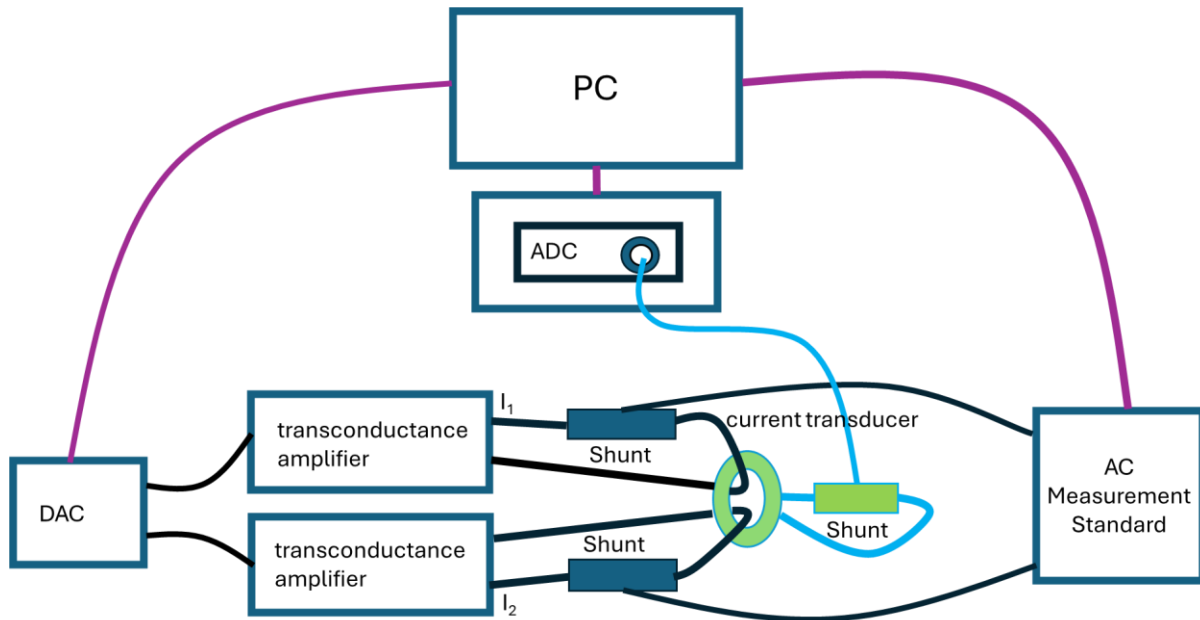
The measurement setup for voltage evaluation is illustrated in the following graphic. In this configuration, the PC manages both the signal generation and the measurement procedure. A digital-to-analog converter (DAC) produces two single-frequency voltage signals on separate channels, which serve to synchronize the phase of the two calibrators. To prevent ground loops, the DAC and calibrators

are electrically isolated using opto-isolators. Each calibrator then generates a single-frequency signal with identical frequency and phase as the corresponding output of the opto-isolator. Finally, the outputs of the two calibrators are combined to form a two-frequency voltage signal, which is subsequently applied to test the PTB measurement system.

An AC measurement standard with two channels was used to alternately measure the output signals of the two calibrators. The measurements were then evaluated to determine whether the combined signal corresponded to the sum of the individually measured single-frequency signals. This comparison served to validate the applicability of the superposition principle to the measurement system.



The verification of the current measurement follows the same principle as the voltage measurement. The corresponding setup, shown in the graphic, employs two transconductance amplifiers to generate two currents of different frequencies separately. Since the amplifiers accurately reproduce the output of the DAC, additional phase control is not required. The output currents of the amplifiers are first measured by the two channels of the AC measurement standard, after which the combined current, consisting of two frequencies, is measured through a zero-flux converter by the PTB measurement system. The validation of the superposition principle is therefore carried out in direct analogy to the voltage measurement.



The measurements have already been completed, including the subsequent careful evaluation of the data. A LabVIEW-based software has been developed to calculate the influence of intermodulation on the overall measurement uncertainty of the system for each individual measurement.

3.4 Task 2.4.4 EMC prediction and design optimization (Lead: SIGN, participants: PLEXIM, XC, TUDE)

Any new electronic LED driver typically takes about 6- 9 months to develop. One of the biggest uncertainties in the design process of electronic converter is the EMC compliancy. Currently this is solved by trial-and-error and most of the time additional components are added to the host system to meet regulation standards. Therefore, the measurements and design are quite time consuming and poses challenges related to regulatory compliance. Therefore, it is desirable to develop a methodology to predict EMC performance at early design phase and support the architectural decisions and design process to enhance the possibility of compliance at the release phase. In this cross-domain topic such an approach is being addressed and following steps were realized:

- Identification of use cases (electrical class, parasitic environment, applicable regulations) of the electronic LED converters.
- Development of simulation models and EMI building blocks to meet EMI requirements at system level (e.g., Luminaire/host with integrated control/converter)
- Development of required templates/tools to implement EMI qualification in standard design flow.

Prediction of conducted emission for 36W driver

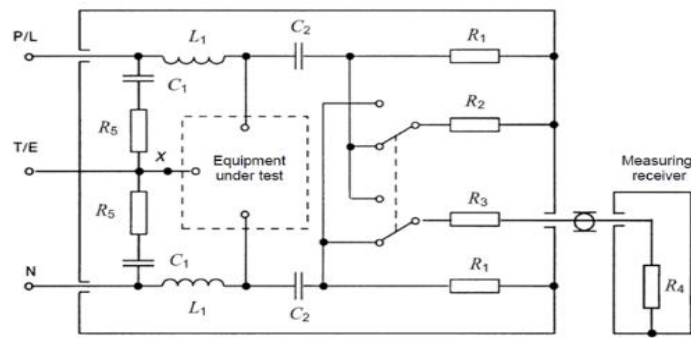


Figure 36: Artificial mains network (AMN)

To create a simulation test bench, it is required to also integrate spice models of measuring equipment. A schematic diagram of an AMN has been shown above. The AMN is used to measure the disturbance on the mains port up to the frequency range of 30MHz. Depending on the application requirements, an electronic power converter can be of different electrical class such as with or without protective earth (PE). There are also variations in the host where such a driver is integrated. The host can be of completely non-conducting material (e.g., plastic) or can be made of metal. In the figure below, this overview in the form of a matrix is presented where different electrical classes of drivers and their integration on hosts are shown. This is an important system level aspect for EMI prediction methodology. This combination of host and converts determines the parasitic environment. The parasitic environment determines the impedance for the mainly common mode and differential mode currents.

Host/Luminaire	Touchable metal parts	Not touchable metal parts	Completely non metallic
Driver with PE	#1a: Pure class I – drier metal body	#5: mostly outdoor	#7: mostly indoor waterproof
	#1b: Pure class I – drier plastic body		
Driver without PE	#6a: Connection with PE	#4	#2 Pure class II
	#6b: No connection with PE		
Driver with PE but with FE	#3: Mostly outdoor (metal, wooden, plastic poles)		

Figure 37: CONVERTER APPLICATION in a Host

Based on the use case definition, an EMI test bench as per CISPR definition has been proposed. An example of such a test bench is presented below. The individual blocks represent different components of the converter used for the purpose of this modelling. For custom designed magnetic components or film capacitors incorporated in EMI filters spice models are usually not provided by manufacturers. In most cases spice models provided by the manufacturer of components were found to not be good enough for use in EMI modelling. Therefore, broadband spice models for critical components have

been created. A test bench incorporating various building blocks has been developed in line with the models presented in Figure 38.

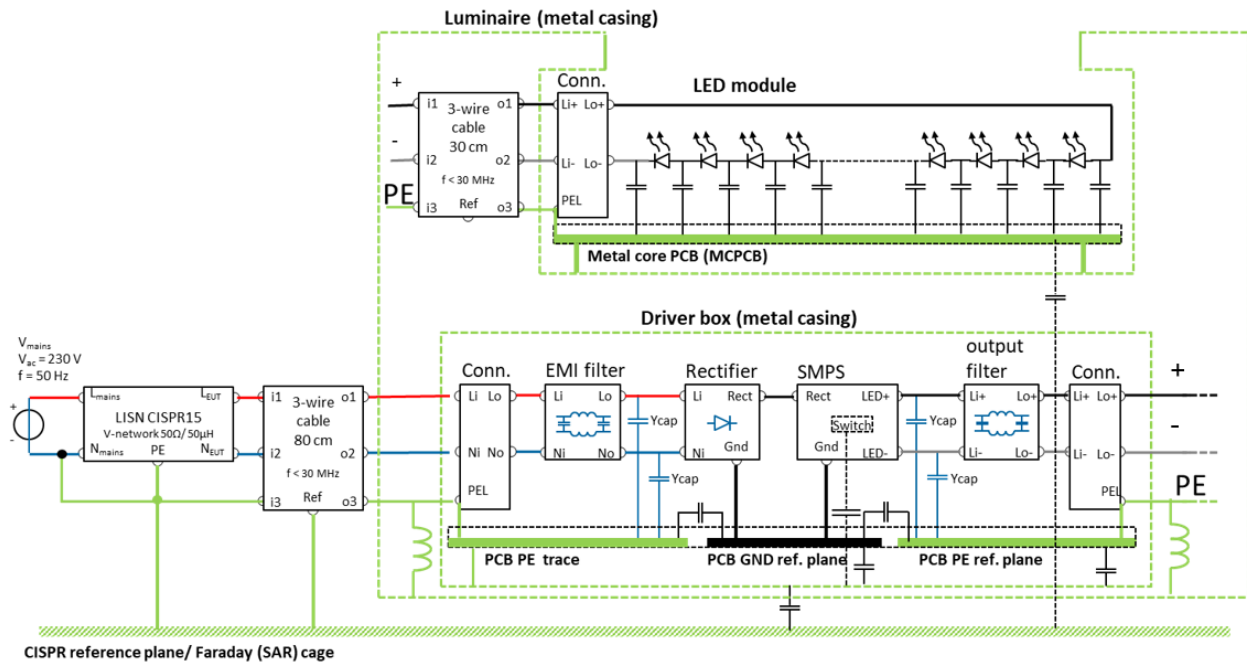


Figure 38 An EMI test bench

The time domain data have been further processed, and EMI spectra have been generated. To validate the simulation results, conducted emission (CE) measurements were carried out. In the figure below a CISPR 15 measurement set-up has been shown. In this Figure, the LED converter unit can be seen mounted on a reference plane and the measurement device; an artificial mains network can be seen on the ground plane.

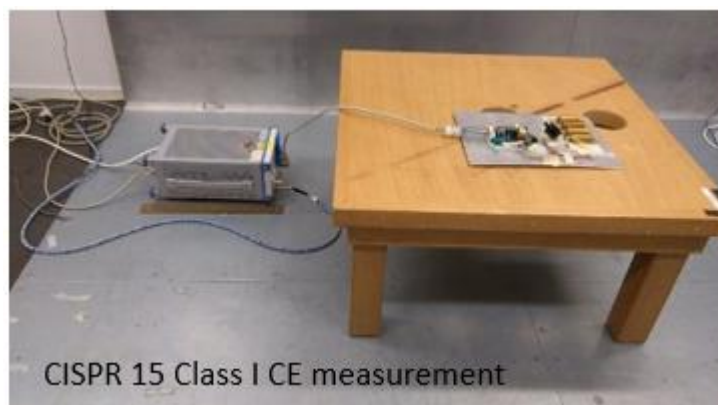


Figure 39 Conducted emission measurement

A comparison of simulated vs measured data is given below in Figure 40. The limit lines for average and peak are also shown in this figure. In general, a good matching of the simulation data with measured data is found. At the lower frequencies, a mismatch can be seen between simulated vs measured data. This can be probably due to the AC electronic power supply and the EMI filters mounted inside EMC chamber used to perform measurements.

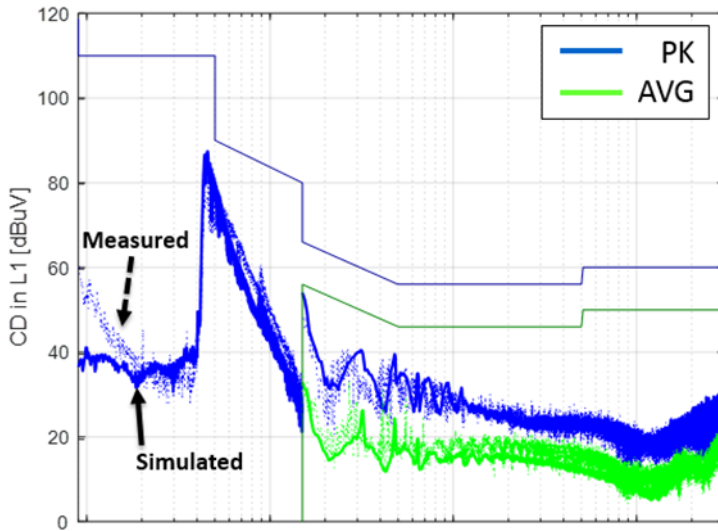


Figure 40 : Simulated vs measurement

Prediction of conducted and radiated emission for 50W driver

Based on preliminary approach to predict emission in the conducted range using an in-house 36 W power converter, modelling has been extended to predict radiated emission in frequency range 30 MHz- 300 MHz for a 50 W power converter. As described above to create a simulation test bench, it is required to also integrate spice models of measuring equipment. A LISN is used to measure the disturbance on the mains port up to the frequency range of 30 MHz. A CDNE is used to measure disturbance on mains or other ports in frequency range from 30 MHz until 300 MHz.

Based on the use case definition (driver with Protective Earth connection), an EMI test bench as per CISPR 15 definition has been proposed below. The individual blocks below represent different components of the converter and have been modelled for the purpose of simulation.

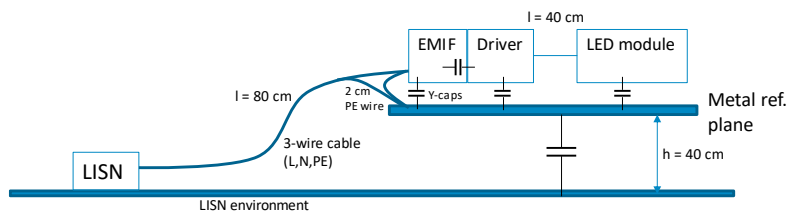


Figure 41 :Schematic of a conducted EMI test bench

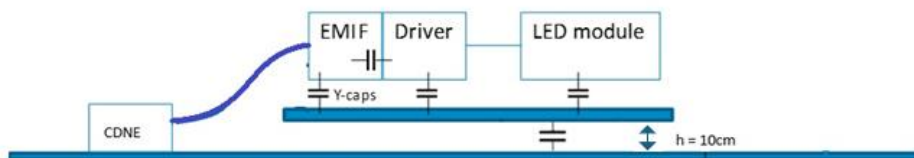


Figure 42: Schematic of a radiated EMI test bench

To validate the simulation results, conducted emission (CE) and radiated (CDNE) measurements were carried out for a 50 W driver.

A comparison of conducted emission (CE) simulated vs measured has been shown below in Figure 43. The limit lines for average and peak have also been shown in this figure. In general, a good matching of the simulation data with measured data can be seen.

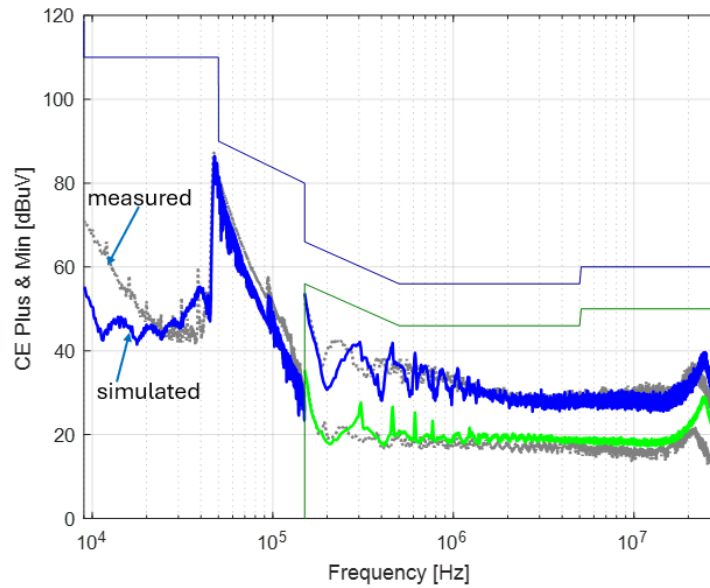


Figure 43: Result comparison 50W driver- simulated vs. measurement

The simulated and measured data for radiated emission (CDNE) have been presented below. In general, a satisfactory matching of the simulation data with measured data can be seen.

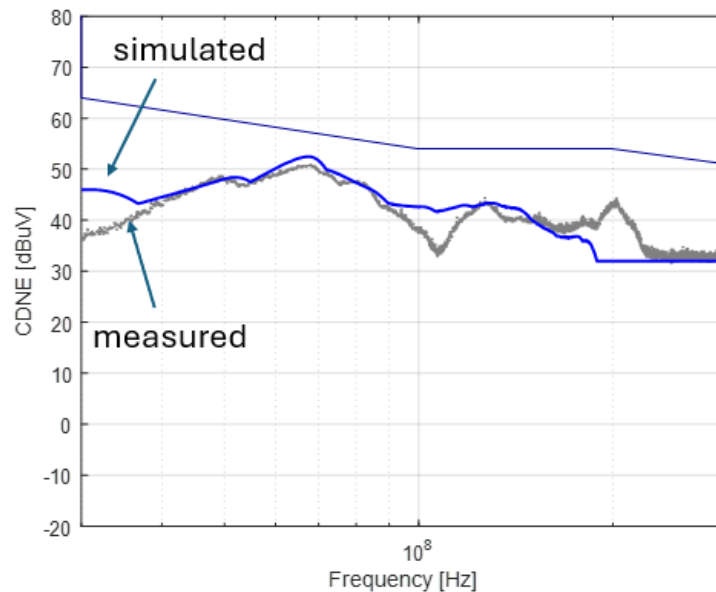


Figure 44: Result comparison CDNE 50W driver- simulated vs. measurement

Mismatches between simulation and measurements results are present due to fact that CDN-E model incorporated in simulation testbench is based on CDN-E diagram with ideal components.

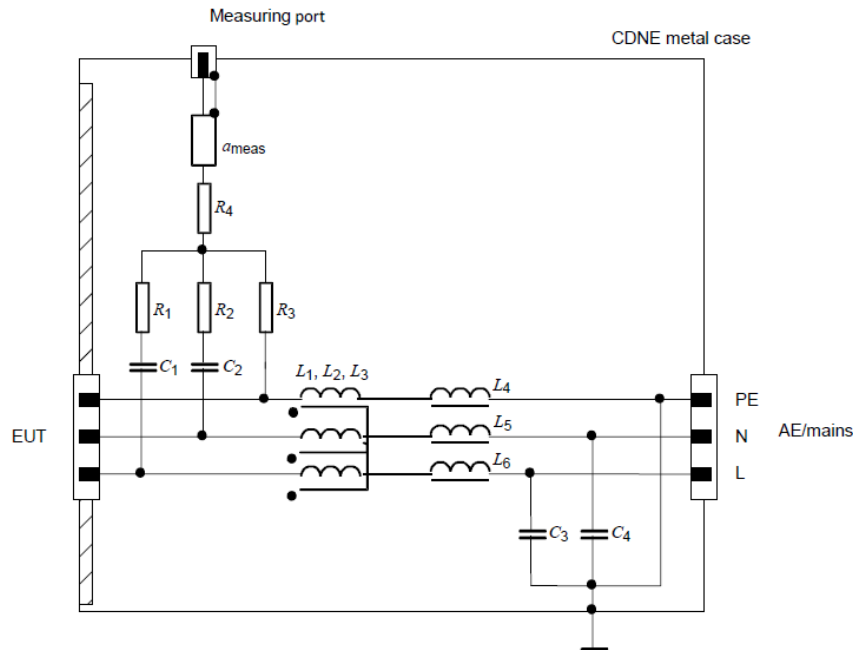


Figure 45: Model of Coupling-Decoupling network- Emission (CDNE)

Common mode impedance at the EUT port of 150Ω cannot be realized with one set of coupled inductors. Coupled inductors are realized by feeding the 3 wires through several ferrite rings. The coupling factor of the HF inductors is not equal to 1. If the coupling is < 1 then the resulting leakage inductance will cause resonance effects in combination with the parasitic capacitors in the CDN-E and the EUT. Resonance effects are not modeled leading to mismatches between measurements and simulation.

EMI study for a Gallium Nitride (GaN)-based power converter

An EMC study has been conducted to build knowledge and understand the EMI behaviour on a fast-switching GaN-based driver. The concerned driver has a two-stage design, with the first stage being a PFC boost stage that generates 400V DC for the secondary stage. The secondary stage is a GaN buck with digital control, where a high frequency GaN switching transistors are used.

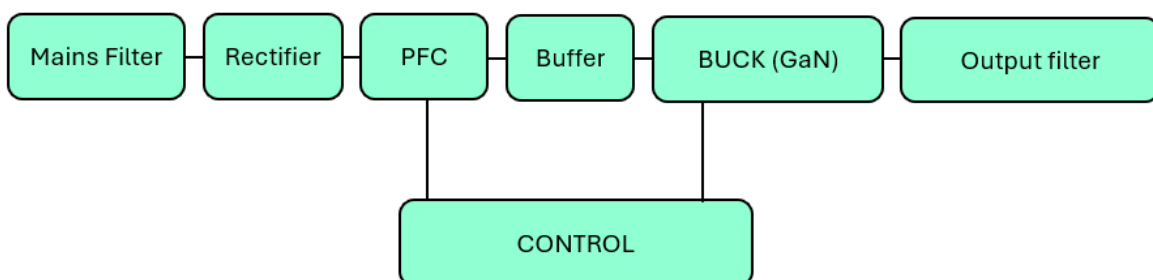


Figure 46: GAN-based power converter topology

The investigation of EMI problems resulting from the fast-switching GaN components involved deactivating the primary PFC stage while keeping the filtering circuit and the secondary buck stage, a GaN devices, active. Subsequently, the secondary stage was supplied with the 400 V DC bus voltage, which it is designed to receive from the PFC stage. GaN driver with a fundamental switching frequency of 800 kHz was considered, in contrast to silicon-based transistors used in power converters for lighting applications, which have typical switching frequencies of 40 kHz. The twenty-fold increase in switching frequency of GaN based power converters, coupled with compact design requirements, results in significantly aggravated EMI issues.

Following steps were conducted for evaluation purpose:

- The prototype converter has been integrated into a host that represents a final product. In a practical scenario, this host must demonstrate compliance with regulatory requirements.
- To investigate the EMI issues caused by fast-switching GaN devices, the primary boost stage was disabled and a DC voltage was applied to the converter’s input. Conducted emission (CE) and radiated emission (RE) measurements were performed by using the CDNE approach as per the set-up described in CISPR15.
- Various measurements were conducted, as shown in Figs. 47,48 and 49, to understand the root cause of EMI failures and the sensitivity of associated coupling paths.

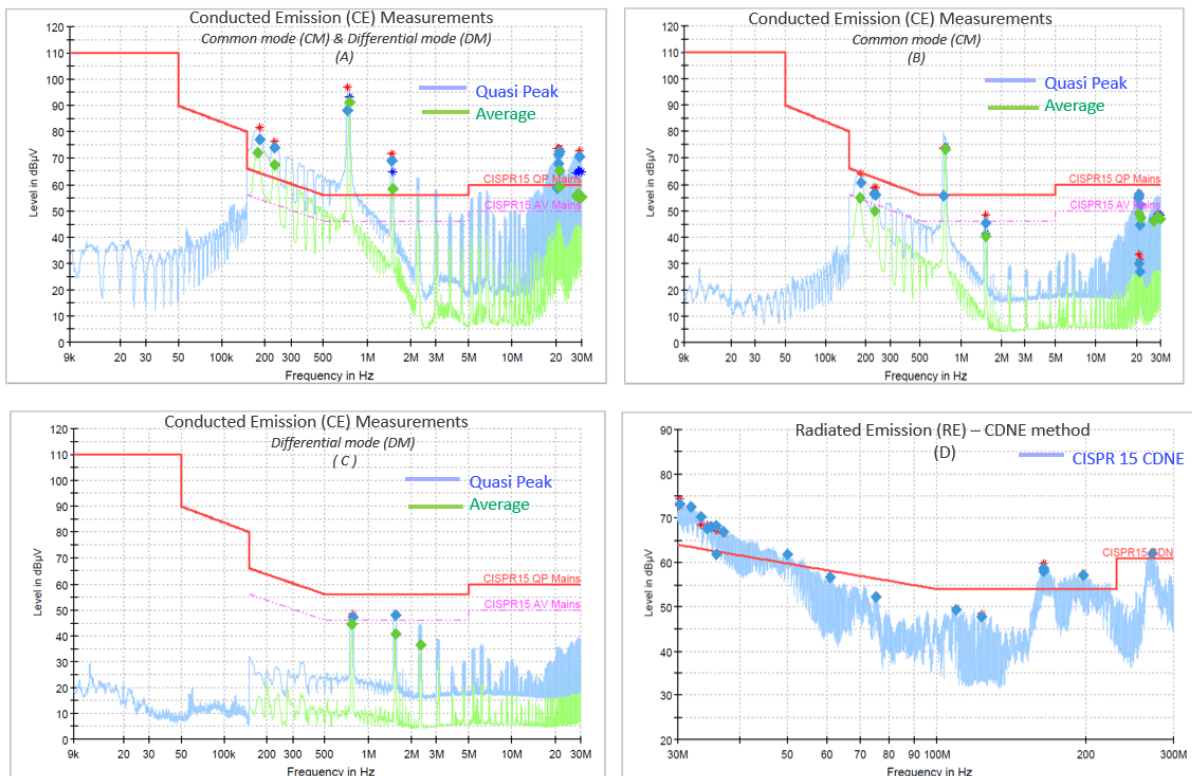


Figure 47: Reference Measurements for Conducted & CDNE, Conducted emission CM+DM(A); Conducted emission: CM(B); Conducted emission: DM(C); CDNE:RE(D)

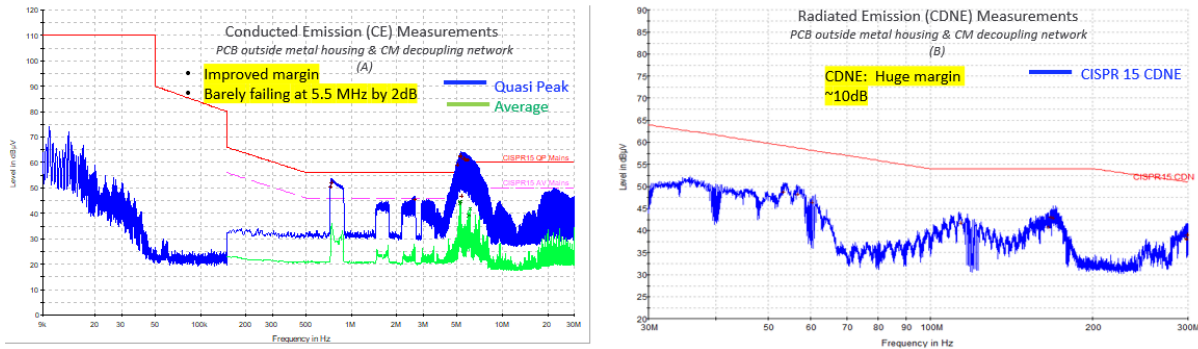


Figure 48: CE & CDNE: PCB outside host & decoupling network applied on mains wire

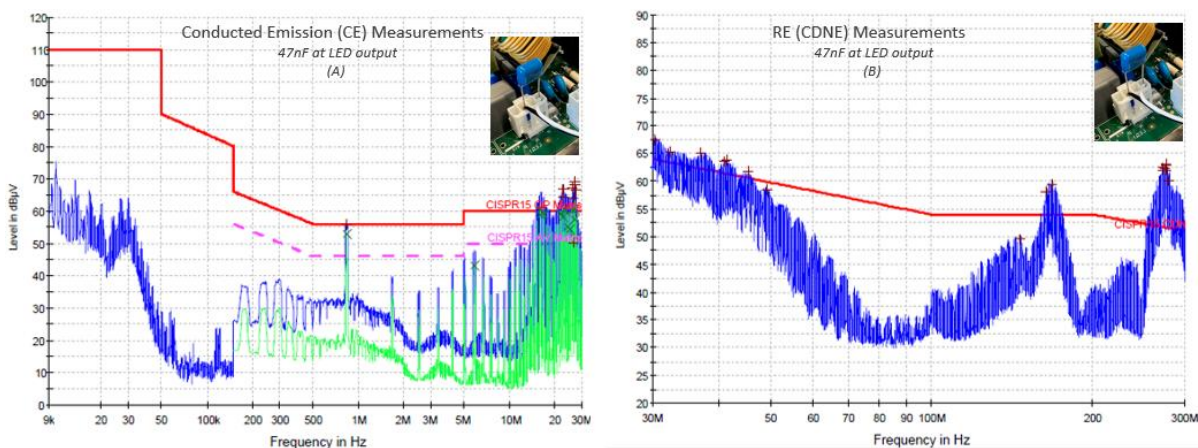


Figure 49: Emission spectrum: CE & CDNE, 47nF X-cap added at the LED output

These findings can lead to better designs or may contribute to improve the EMI performance for future designs where high speed switching components are used. A full paper describing our approach has been published in the IEEE PEMC conference:

<https://ieeexplore.ieee.org/document/10726402>

EMI for 3-stage interleaved 1800W PFC

The simulation test bench to predict conducted emission for an electronic driver was used to design and optimize an EMI filter for the 3-stage interleaved 1800W totem-pole PFC circuit studied in UC 2.3. Conventional PFC converters use a passive diode bridge for rectification. However, the disadvantages are significant power losses, which results very often in bulky heat sinks and heat dissipation. To achieve higher efficiency wide-bandgap semiconductors can be incorporated to move toward a bridgeless architecture. To realize 1800W PFC 3-stage interleaved continuous-conduction mode (CCM) totem-pole PFC circuit was developed in UC 2.3. The simulation test bench to predict conducted

emission for an electronic driver was used to design and optimize EMI filter for this new topology. The simulated data have been presented below.

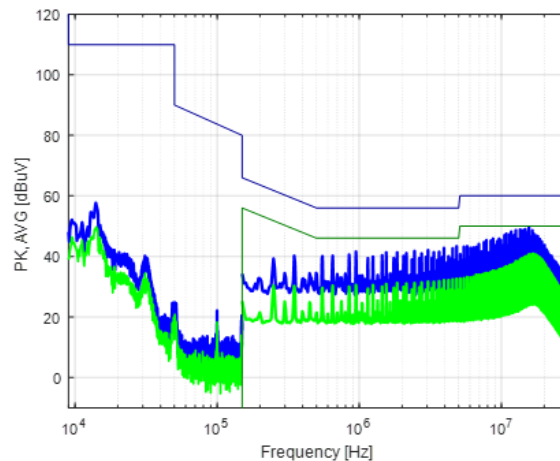


Figure 50: Simulated conducted emission for 1800W PFC

4 Conclusion

4.1 Contribution to overall picture

The following gives an overview of the contributions and main activities done:

AIT

AIT's main activity was the develop of the automated testing and reporting HIL environment. For the selection of the test cases and requirements there was a close exchange with Task 3.2.3 and UC2.3. The testing and reporting environment supported Task 3.2.3, especially the benchmarking of the different topology for LED driver and LV DC distribution grid. Additionally, AIT designed, assembled and tested an LED driver prototype with a flying capacitor topology.

Since tasks 2.4.1 and 2.4.2 are closely related, AIT participated in the testing and reporting of the software developed as part of task 2.4.2.

PLEXIM

PLEXIM's contributions to WP2.4 have been central to the digital transformation of power electronics design and validation within PowerizeD.

Through the development of the Target Support Package (TSP) and the SPICE-like solver, PLEXIM has established an integrated toolchain that connects high-level modeling, automated code generation, and detailed electrical simulation.

These developments have:

- Accelerated controller prototyping and reduced development time by more than half
- Bridged the gap between idealized system simulation and detailed device-level analysis

Beyond the technical achievements, PLEXIM's work contributes to strengthening Europe's expertise in advanced simulation and control design. The developed methodologies and models provide a lasting foundation for continued research, education, and industrial application in intelligent power-electronics design.

VSL

VSL's recent work has focused on refining efficiency measurement techniques and assessment tools within the project. Their efforts have enhanced the accuracy and reliability of system efficiency verification and validation, contributing significantly to improved performance and compliance. By pursuing rigorous testing methodologies, VSL continues to drive advancements in precision measurement, laying the groundwork for future best practices in the field of efficiency measurement of power electronics.

UTWENT

UTWENTE has played a pivotal role in the development and validation of efficiency measurement methods, exemplified by their innovative use of the calorimeter for precise power loss measurements. The calorimeter enabled highly-accurate and repeatable assessment of losses in power converters and components, which is essential for modern power electronics applications. The novel measurement approach applied in the calorimeter has resulted in unprecedented accuracies, which not only improved the reliability of assessment tools but have also supported the project's broader objectives.

ZES ZIMMER

A prototype wideband voltage divider was developed with excellent wideband characteristics. This divider is well suited for measurement of higher frequency voltage signals, up to 150 kHz. Work instructions and manufacturability for possible series production of the voltage divider were developed and tested with success.

PTB

The PTB has developed two measurement systems for the wideband evaluation of voltage and current sensors. A unique property of the PTB measurement system is that it ensures a systematic assessment of the additional uncertainty contributions and allows a more precise validation of the system's performance when it is used to measure multi frequency signals.

SIGNIFY

Signify's EMC evaluation activities focused on analysis and exploring use cases where predictive approaches for electromagnetic interference (EMI) add value, particularly in the context of regulatory compliance. A preliminary method to predict conducted emissions was developed and validated using a 36W LED power electronics converter, which was later extended to a 50 W converter. This approach was further refined to predict radiated emissions within the frequency range of 30 MHz–300 MHz for



the same 50 W converter. Models for measuring equipment, including Line Impedance Stabilization Network (LISN) and CDN-E (Coupling-Decoupling Network), were created and integrated into a simulation test bench. Additionally, simulation data in time domain were converted to be aligned with CISPR sampling requirements, ensuring compliance with resolution bandwidth standards. Validation of simulated EMI data was carried out through measurements, strengthening the reliability of the predictions.

An EMC (Electromagnetic Compatibility) study was conducted to understand EMI behavior in a fast-switching GaN-based power converter. The simulation test bench for conducted emission prediction was also utilized to design and optimize an EMI filter for a 3-stage interleaved 1800W totem-pole Power Factor Correction (PFC) circuit, demonstrating its practical application in circuit design and compliance enhancement.

4.2 Relation to the state-of-the-art and progress beyond it

XMC Target Support Package

The XMC Target Support Package (TSP) advances beyond the state-of-the-art by bridging high-level model-based design in PLECS with direct automated code generation for Infineon XMC microcontrollers. Unlike traditional manual coding approaches, it integrates advanced peripheral support, safety features, and compatibility with DAVE and ModusToolbox, enabling faster prototyping and reducing development time by over 50 %. This makes embedded control development more robust, efficient, and widely accessible across power electronics applications.

SPICE-like Solver

SPICE-like solvers are a cornerstone of power electronics simulation, but traditional implementations depend on proprietary device models that require significant effort to implement and maintain. Recent advances such as platform-independent languages (Verilog-A) and standardized interfaces (OSDI) aim to ease model portability and bridge research with system-level applications.

In numerical methods, classical trapezoidal and BDF schemes remain standard, though newer one-step methods show potential advantages in certain scenarios.

The new solver developed within PowerizedD builds on this state-of-the-art by offering a mixed-formulation approach that unifies PLECS and SPICE simulations, a higher-order solver for improved robustness, advanced netlist import with error detection, and a user-friendly GUI. These features represent a significant step towards a more versatile and accessible simulation environment for power electronics engineers.

Calorimeter

Calorimeters are the instruments of choice for measuring the efficiency (losses) of high-efficiency power electronics. They are more accurate than electrical methods since calorimeters measure the losses directly. Present state of the art calorimeters typical have an accuracy of 1 % for losses in the 20-100 W range, that is increasing to 2 – 5 % accuracy for losses below 10 W.

A key progress beyond this state of the art realized in the PowerizedD project is the development of a calorimeter with a novel measurement approach where the loss of a device under test is directly compared to the loss of a reference heater. This approach makes the calorimeter less sensitive to heat



leaks to the environment. Following several implementation revisions, a final version of the calorimeter was developed with an accuracy of better than 0.5 % for losses of 10-100 W.

EMC

With the growing demand for high-power applications, various electronic converter topologies employing higher switching frequencies are increasingly being utilized. This approach is primarily adopted to maintain high efficiency and minimize the form factor. However, this trend results in a significant increase in challenges that must be addressed to ensure compliance with EMC regulatory requirements. To tackle these challenges, a methodology for predicting EMC performance and defining corresponding integration design rules has been developed.

The test bench created as part of this effort was successfully utilized to design and optimize the EMI filter for a 3-stage interleaved 1800 W totem-pole PFC circuit studied in UC 2.3. Based on the simulation results, design and integration guidelines were formulated and transferred to the project team responsible for the relevant topology.

4.3 Impacts to other WPs and Tasks

Tasks 2.4.1 and 2.4.2 are closely linked: the test system from 2.4.1 provides preliminary testing of the software developed in 2.4.2 using a Hardware-in-the-Loop (HIL) setup before field trials. The Task 2.4.1 impacted UC 2.3 LED driver to demonstrate the potential of automated HIL testing the reporting environment. Based on the automated simulations and reports, the topology selection process was further simplified.

The tools developed in Task 2.4.2 directly support other project activities. The TSP has been validated in Task 2.4.1 and shaped by requirements from UC2.3 and CDT4.1, ensuring broad applicability for control prototyping. The SPICE-like solver is being applied in UC1.6a, UC1.6b, and UC2.3, where accurate modelling of non-ideal effects is essential.

Both subtasks mainly address UC2.3 in WP3 and CDT4.1, CDT4.2, and CDT4.4 in WP2. In WP2.4.3, new efficiency measurement equipment have been applied in the final project year to evaluate the efficiency of the new power electronics developed in the UCs. Regular online and in-person meetings have been conducted with the respective UC leaders to ensure that the tools developed in WP2.4.3 meet their requirements. The EMC prediction methodology depends on both UCs and CDTs: hardware requirements rely on UC2.3, while alignment with the software tool requires CDT4.2.

4.4 Contribution to demonstration (what aspects of the work that will be demonstrated)

The UC2.3 LED driver illustrates the capabilities of automated C-HIL testing and reporting during development, prior to field validation. The setup has been used to benchmark multiple multi-level topologies, with results presented at PCIM 2024 [2]. Benchmarking identified the three-level flying capacitor cell (FCC) as the most promising topology, providing a reference for component-level resource prioritization. As part of this activity, the Target Support Package (TSP) developed by PLEXIM was employed to generate and verify the digital control code for the Infineon XMC microcontrollers used in the UC2.3 prototype. The TSP enabled rapid iteration between modelling, simulation, and embedded implementation within the automated HIL setup.



The underlying methodologies and technologies are adaptable to other applications, and the performance of both electrical and calorimetric efficiency measurement setups have been validated across multiple project use cases (UC 1.6c, 2.2, and 2.3).

4.5 Other conclusions and lessons learned

An important conclusion from this project is that hardware-in-the-loop (HIL) simulations have proven to be an extremely effective tool for selecting the appropriate system topology for Task 3.2.3 and UC2.3's. The ability to test different configurations in a controlled and repeatable environment enabled a more reliable and data-driven decision-making process early on in the design phase.

However, HIL also has its limitations; it may not be able to fully replicate all dynamic behaviors or system latencies of the real prototype. For example, there are differences between C-HIL and laboratory testing when it comes to control dimensioning.

A further insight is that innovative, high-precision measurement techniques for assessing power converter efficiency can play a pivotal role in advancing power electronics design and application. Moreover, incorporating EMC modelling early in the design process can yield critical understanding of the electromagnetic behaviour of new converters, resulting in lower development costs and shorter time-to-market. However, it is also clear that meaningful simulations of high-frequency effects depend on broadband component models, which may not yet be available at the initial design stages.



5 References

- [1] L. Jol and G. Rietveld, "Improved Sampling Wattmeter for Low Frequencies (45 Hz-55 Hz)," IEEE Transactions on Instrumentation and Measurement, vol. 53, no. 4, pp. 1234-1240, Aug. 2004.
DOI: 10.1109/CPEM.2004.305581

- [2] K. Machtinger, P. Jonke and U. Boeke, "Comparison of Multi-level Topologies to Reduce the Components Voltage Stresses when Powered from Industrial DC Grids," PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, Germany, 2024, pp. 2114-2122.
DOI: [10.30420/566262299](https://doi.org/10.30420/566262299)

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