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PowerizeD

Digitalization of Power Electronic Applications within Key Technology Value Chains

Deliverable	**Summary report on results on Cross Application & Domain Topics of methods for intelligent sensing and control**		
Involved WPs	WP2.3	**Deliverable type**	Public
Project	PowerizeD	**Grant Agreement Number**	101096387
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V	**Date**	**Author**	**Description**
1	19.02.2025	Alessandro Portesan, Luca Gagliano, IFI	Intermediate Report
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3	10.11.2025	Dirk Rudolph, TUDD, and others	Internal Review
4	12.11.2025		Final check and submission

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1 Introduction & Scope

1.1 Purpose and target group

Deliverable D2.3.5: “Summary Report on results on Cross Application & Domain Topics of methods for intelligent sensing and control”. Dissemination level is “public”.

The Deliverable was updated and reviewed by CDT project partners.

1.2 Contributions of partners

Intelligent sensing and control consist of the two CDTs 3.1 and C3.2 (see Table 2).

Table 1: Theme Intelligent Sensing and Control separated into two Cross Domain Topics

Domain	Leader	CDT Title
CDT 3.1	TUDD	SW-related Control Approaches
CDT 3.2	IFI	HW-related Sensing and Control Approaches

During Reporting Period 1, we reorganized the internal structure of the work. During Reporting Period 2, we had only minor updates: the updated structure is displayed in table 1. The workgroup “Digital twin for a MOSFET” by TUDO had a change of scope and is renamed “SiC gate driver advanced protection”. It still includes the evaluation of a digital twin. The CDT3.2 now also includes the workgroup “Monolithically integrated SiC sensors” by TU Delft.

Table 2: Updated task description and related partners

Task Name	Responsible	CDT 3.1	CDT 3.2	TUDD	IFI	EDI	TUDO	FPG	DUTH	PLEXIM	RISE	KTH	ALSTOM	HEPO	XC	TU DE	Work-group
dvdt control	TUDD (Tristan Eberle)	x	x	R	C	C	C										1
On-state voltage	TUDD (Tristan Eberle)	x	x	R		C											1
GDU interface	IFI (Alessandro Portesan)	x	x	C	R				C								2
Transient thermal impedance	TUDD (Matthias Meißner)	x		R													
Sensor data	TUDO (Christoph Schmickler)	x	x	C	C	C	R										1
Advanced protection	IFI (Alessandro Portesan)	x	x	C	R				C								2
SiC Gate Driver Advanced Protection	TUDO (Christoph Schmickler)	x	x				R			C	C						3
Self-adaptable GDU	KTH (Hans-Peter Nee)	x	x		C						C	R					4
Smart GDU for BEHDV	KTH (Hans-Peter Nee)	x	x		C							R					4
Energy harvesting	RISE (Cristina Rusu)	x	x								R		C				5
Adaptive PWM control	FPG (Georg Heiland)	x	x					R									
State and health analyzing	FPG (Georg Heiland)	x						R						C			6
Multirate	XC (Stephan Corban)	x													R		
Monolitically integrated SiC sensors	TUDE (Zhenhua Z. Zhang)		x													R	

1.3 Relation to other activities in the project

WP2.3 contributes to a series of use cases: UCs: 1.1, 1.4, 1.5, 1.6a, 1.6b, 1.7, 2.3, 2.4, 3.1a, 3.1b. The partners independently manage their collaborations according to the overall plan, then report their progress in our WP2.3 status update meetings.
Each workgroup lead shares their contribution to the WP2.3 status report, which is stored in

PowerPoint format on the project cloud for easy consultation by all partners. At each WP2.3 meeting the status report is updated. Partners give special focus to the status of their collaborations with each partner and to the novelty of their work.
With this setup, partners within WP2.3 are therefore constantly updating each other. WP2.3 lead then updates WP2 lead on the status, progress, risks, collaborations and novelty of the work done.
The partners use this status report as a base to produce their reports in written format for the overall PowerizeD report.

2 Final Results

2.1 Contribution to overall picture

Early in the project, we have defined the motivation and key objectives of our work in Intelligent Sensing and Control.

Table 3: Motivation and Objectives of the WP2.3 Intelligent Sensing and Control

Motivation and Objectives
The gate driver should be intelligent. It should be able to: • Protect the power semiconductor (short circuit, overcurrent, SoA) • Optimize the switching behaviour (efficiency, EMC…) • Adjust the on-state voltage in a limited range to simplify module parallelization The gate driver should be simple: • Get rid of sensitive analog interfaces and implement a new digital interface

We have charted the work to be done. We defined workgroups and individual tasks.

Table 4: Definition of workgroups and individual tasks, indicating planned result and impact

Methodology and Innovation	CDT Solution Providers	Planned Result and Impact
1. Sensor data and control of the semiconductor behaviour	TUDD, IFI, EDI, TUDO	Control behavior of power switches and sensing operating conditions
2. Gate driver interface and advanced protection	IFI, TUDD, DUTH -> ABB	Develop intelligent GDU for power modules
3. Gate driver with advanced protection	TUDO, KTH	Concept for a gate driver with advanced protection, diagnostics and control function
4. Smart self adapt. GDU and GDU for BEHDV	KTH, IFI, RISE	Develop smart GDU concept suited for BEHDV and traction inverter
5. Energy harvesting	RISE, ALSTOM	Feasibility study for harvesting energy for new/ improved sensors
6. Battery state and health analyzing	FPG, HEPO	Extend the SW functionality by data analysis of battery health data
Ind. Task 1: Transient Thermal Impedance	TUDD	Predict module failures using transient thermal impedance during operation
Ind. Task 2: Adaptive PWM control	FPG, HEPO	Minimize losses in a buck-boost converter circuit by adaptive PWM control
Ind. Task 3: Multirate control	XC	Ultra-high bandwidth multirate control scheme and hardware based on FPGA
Ind. Task 4: Monolitically integrated SiC sensors	TUDE	SiC reactive ion etching process development for sensor integration

Key achievements are the development of concepts and prototypes for dynamic and static control of Power Switches, using advanced gate drive technologies with different approaches. Results from demonstrators showcased improved performance in terms of EMI and power losses.

The key contributions to deliverables submitted in Reporting Period 2 are:

1. Prototyped advanced switching control approaches and demonstrate energy loss reduction up to 45%
2. Built a fully integrated smart DAB converter for Off board charger applications
3. Contributed to sensing advancement, including thermal energy and transient thermal impedance measurement
4. Performed investigations into new control methods suited for high frequency and wide bandgap switches
5. Successful demonstration of two different battery charging methods and their influence on state-of-health
6. Implemented neural network in a digital controller which is able to detect the grid state and load type
7. Demonstration of turning a hard-switched topology into a ZVS switching device

2.2 Relation to the state-of-the-art and progress beyond it

In WG1, TUDD developed a Class B output stage based on MOSFETs. By introducing a precisely defined bias voltage, the typical crossover distortion of several volts known from conventional Class B amplifiers could be almost completely eliminated, ensuring that the output voltage follows the input signal without a dead band. This concept allows a straightforward implementation of the Class B amplifier without requiring any software-side compensation of crossover distortion.

To further improve the dynamic performance, the discrete digital-to-analog converter (DAC) was optimized for high-speed operation. A PWM period of 20 ns can now be achieved. Additional capacitances were integrated into the DAC design to smooth the gate voltage ripple during the IGBT conduction phase.

The overall design has been significantly improved in compactness and robustness, including enhanced thermal management and protection features. These developments complete the intended functionality of the intelligent gate driver as foreseen in the project.

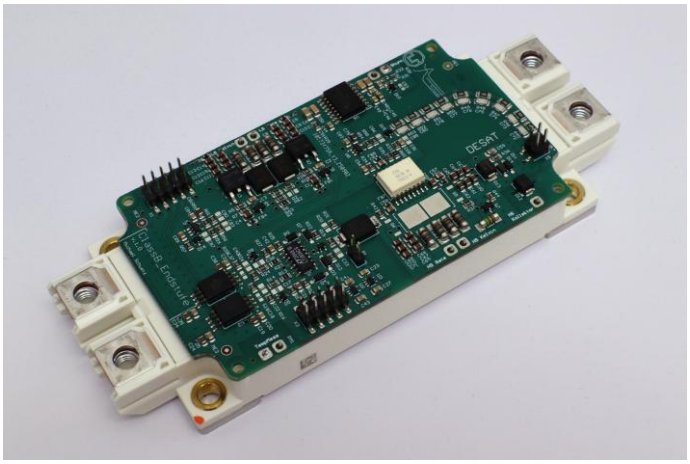


FIGURE 1: DEVELOPED GDU WITH CLASS B OUTPUT STAGE

With the current version, the switching behaviour can be precisely controlled: both dv/dt and di/dt can be actively adjusted during the switching event. This not only enables a controlled shaping of the switching transients but also provides an additional means to balance parallel-connected IGBT modules more accurately.

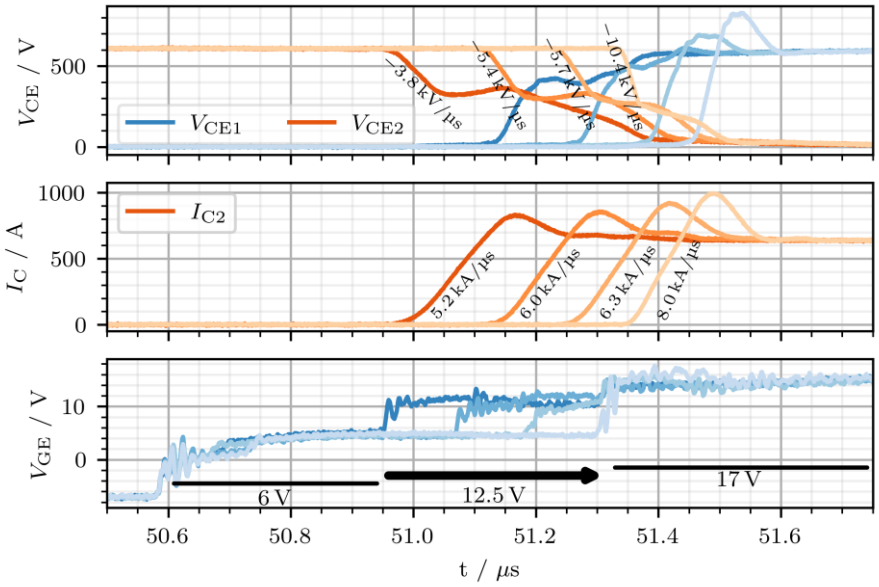


FIGURE 2: DIFFERENT GATE VOLTAGE TRAJECTORIES TO ADJUST THE SWITCHING BEHAVIOR

These advancements form the technical basis for influencing the switching and conduction characteristics as well as for achieving current balancing within the UC3.1b use case.

In WG1, EDI developed sequential lowest segment extraction (SLSE) and extended SLSE algorithms for determining optimal gate current profiles for SiC MOSFETs to minimize switching losses while maintaining predefined current/voltage overshoot or dv/dt thresholds. For this purpose, a double pulse test circuit incorporating a gate current source $i_p(t)$, which generates a sequence of pulses defined by the integer parameters n_1, m_1, n_2, m_2, n_3 and n_4, m_4, n_5, m_5 for the turn-on and turn-off phases, respectively (as shown in Fig. 1), was used for simulations. The objective was to identify the parameter combinations that yield the lowest possible switching losses while satisfying the specified overshoot or dv/dt limits.

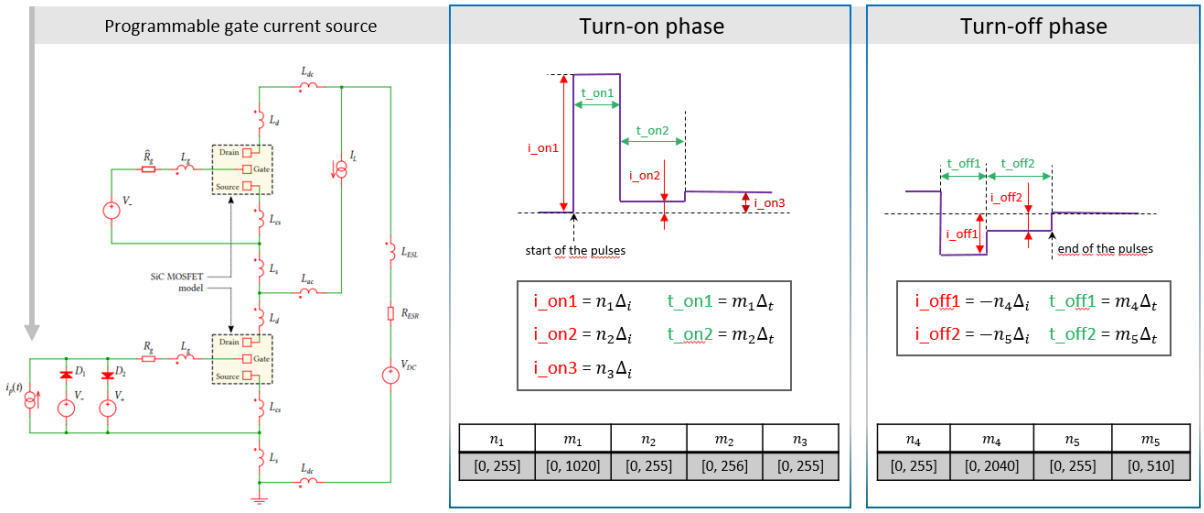


Figure 1: Double pulse test circuit and a sequence of pulses generated by the gate current source.

By selecting the parameters $n_1 = 255$, $m_1 = [15, 16, \dots, 90]$, $n_2 = [0, 1, \dots, 20] \cup [22, 24, \dots, 30] \cup [35, 40, \dots, 60] \cup [70, 80, \dots, 200] \cup [215, 230, \dots, 245] \cup [255]$, $m_2 = [1, 2, \dots, 45]$, and $n_3 = 255$,

a total of 171000 possible (n_1,m_1,n_2,m_2,n_3) combinations were generated for the turn-on phase and simulated in SIMetrix, yielding the results shown as grey points in Fig. 2. The optimal trade-off between the drain current overshoot I_o and the switching loss (denoted as energy loss E_l) is illustrated by a set of points forming the red boundary called the Pareto curve. The black line represents I_o and E_l for a classical gate driver (CGD), which applies a pulse voltage source (instead of the digital current source) to the transistor gate through the resistor R_g, whose values increase from 0.2 to 35 Ω as the line descends from left to right.

As follows from Fig. 2, the advanced gate driver (AGD) is capable of achieving lower I_o and E_l values in comparison to the CGD. However, the question remains of how to efficiently determine the optimal gate current profiles without performing an excessive number of simulations.

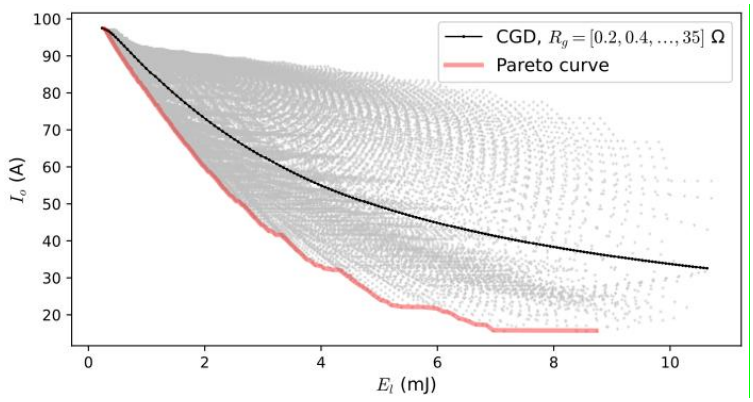


Figure 2: Results (grey points) of energy loss E_l versus drain current overshoot I_o obtained from 171000 simulations conducted at $V_{DC} = 850$ V, $I_L = 180$ A, $T = 140$°C.

The answer to this question is provided in [1], where the SLSE and ESLSE algorithms are introduced, demonstrating that the optimal gate current profiles can be identified by systematically varying parameters m_1, m_2 and n_4, m_5 for turn-one and turn-off phases, respectively. For example, by running only 483 simulations, ESLSE algorithm was able to find 82 optimal gate current profiles, providing I_o and E_l values as shown in Fig. 3 by the red points.

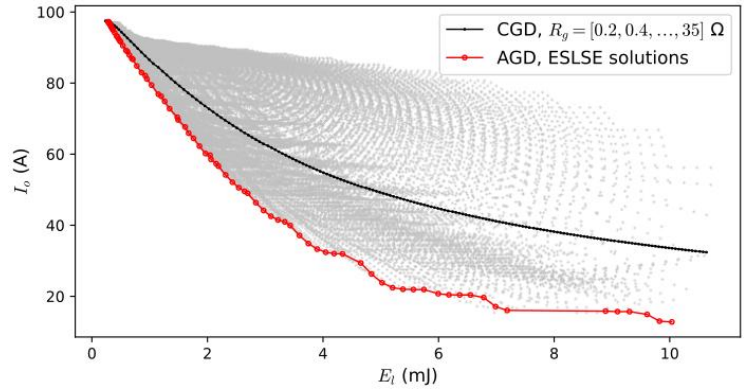


Figure 3: I_o and E_l values corresponding to the identified optimal gate current profiles using ESLSE algorithm.

Different circuit conditions (DC-link voltage V_{DC}, load current I_L, MOSFET's junction temperature T) yield different Pareto curves. Few examples in the energy loss versus maximum dv/dt plane are shown in Fig. 4, where two V_{DC} and three I_L values of 350 V, 850 V and 30 A, 100 A, 180 A were used for the turn-on (on the left) and turn-off (on the right) phases.

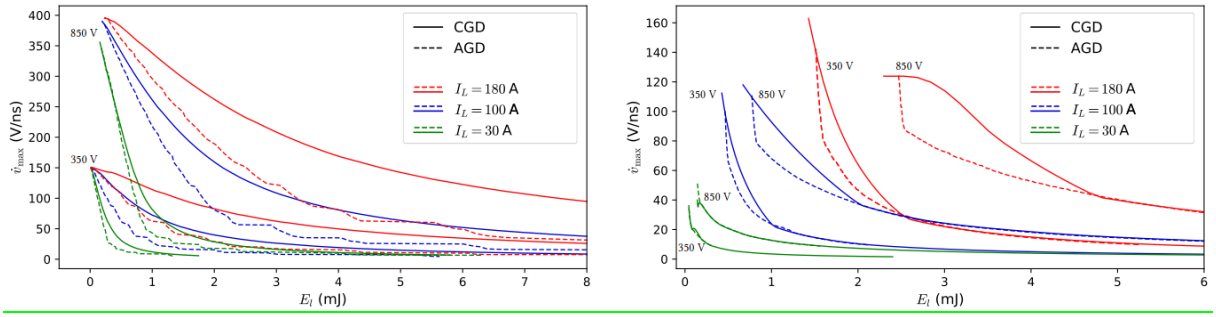


Figure 4: Optimal trade-off curves between E_l and maximum dv/dt values for the turn-on (left) and turn-off (right) phases at different values of V_{DC} (350 and 850 V) and I_L (30, 100, and 180 A), and constant T = 175°C.

To compare E_l values between the AGD and CGD, the following energy loss reduction formula was used:

$$\varepsilon_\vartheta = \left(1 - \frac{E_l^{AGD}|_{\dot{v}_{\max}=\vartheta}}{E_l^{CGD}|_{\dot{v}_{\max}=\vartheta}}\right) 100\%,$$

where ϑ denotes the chosen $\dot{v}_{\max}$ =max(dv/dt)[10] value at which the energy losses were measured. By selecting the targeted $\vartheta = 20$ V/ns, the resulting ε_ϑ values for various combinations of V_{DC} and I_L are shown in Fig. 5. The left side assumes a CGD with adjustable gate resistance, whereas the right side corresponds to a fixed resistance CGD configuration.

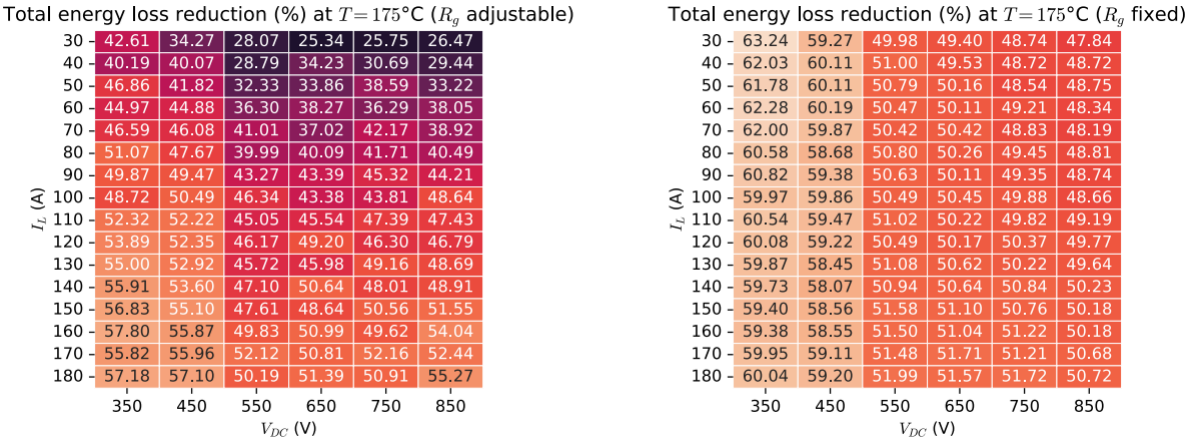


Figure 5: Total energy loss reduction ε_ϑ for different combinations of V_{DC} and I_L. Left: CGD with adjustable R_g values; right: CGD with fixed R_g values – one for turn-on and one for turn-off.

As the simulation results indicate, switching losses can be reduced by up to 63 %, thereby meeting the KPI target of at least 50 %.

[1] R. Shavelis, K. Ozols, M. Ebli and C. Ohms, “Optimization of Gate Current Profiles for SiC Power MOSFETs With Respect to Switching Loss, Overshoot, and Slew Rate”, submitted for review and publication in IEEE Access on 17/10/2025.

In **WG2, IFI, TUDD, DUTH** are working to support two use cases.

For **UC1.6b**, a Smart Integrated Power Module is being developed to build a DAB (dual active bridge).

First prototype has been developed together with **ELC** and **IFAT** and characterized by **ELC.** Final design and layout of the modules done. Characterization done by ELC, together with system level integration, in the Off board charging station.

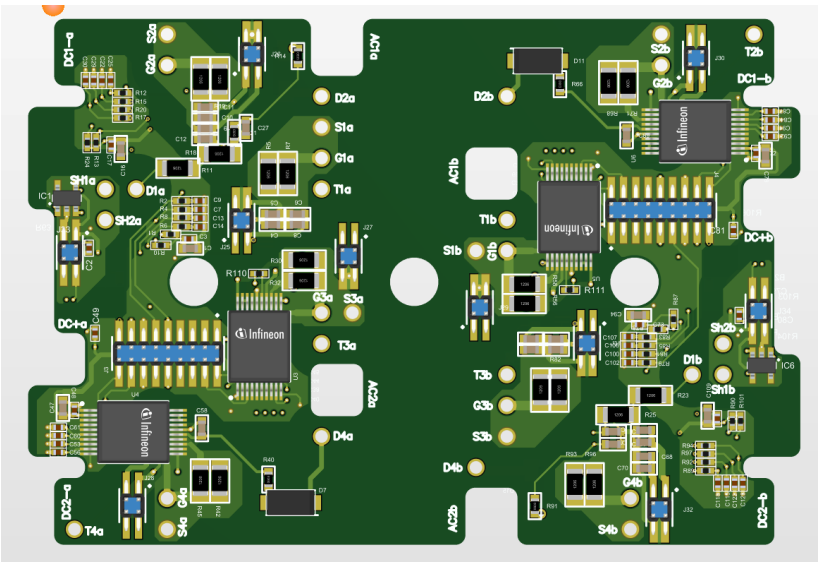


Figure 6. Gate driver unit for integrated module in DAB converter.

Connect to requirement of **UC3.1b,** the objective of IFI was to demonstrate and validate a novel Gate Driver Integrated Circuit (GD) capable of adjusting the dynamic switching behavior of a power device independently of load conditions. This gate driver enables a reduction in switching losses and mitigates electromagnetic interference (EMI). A user-configurable demonstrator platform has been built, enabling the application of arbitrary gate-drive profiles to the power device under test. The gate driver operates as a current source, providing a programmable gate current to shape the switching dynamics. The setup is tailored for Double-Pulse (DP) characterization and has been evaluated in two distinct configurations and across two power-switch technologies. Demonstrator is shown in figure 7

The Gate driver is tested with two different output modes: constant current level and multilevel current level.

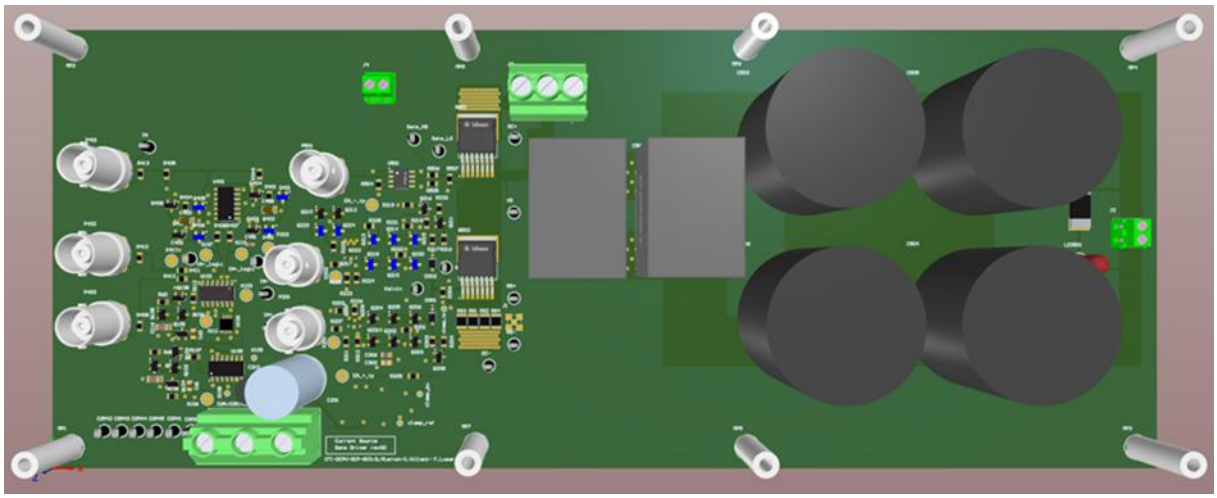


Figure 7 Demonstrator board with advance current source gate driver.

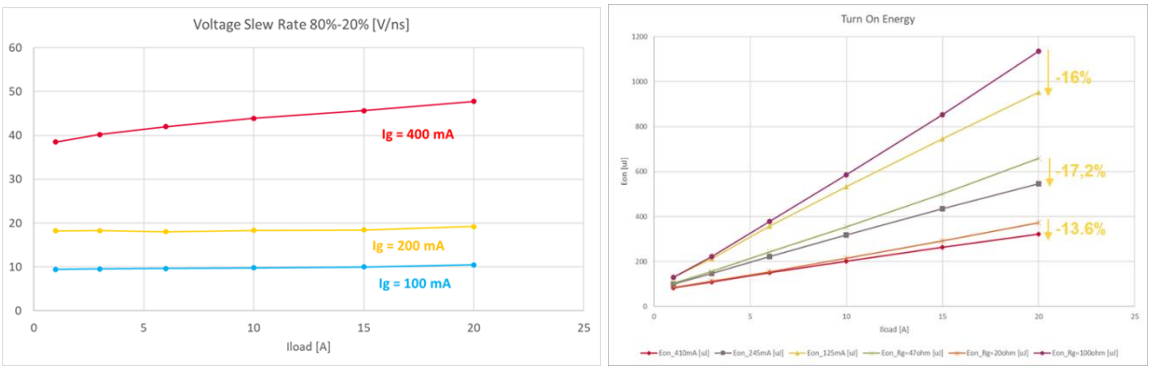


Figure 8 Characterization result of Advance GD with SiC MOSFET, (a) dV/dt remains flat over the load range, (b) comparing with Rg driving, it results in an Eon decreases.

Results are presented in figure 8, the voltage slew rate (dv/dt) remains essentially constant across the entire load-current range up to the device's nominal current for switching speeds at or below 20 V/ns. At higher switching speeds, controllability degrades due to recovery-charge effects. Compared with a conventional gate-resistor (Rg) drive, the single-level current-source gate drive reduces switching losses by up to 17%. (figure 8b).

Eventually, the single level current source driving has been tested with IGBTs. However, Figure 9 shows that controllability is not as good as per SiC MOSFET and the reason is due to fact that IGBTs are characterized by much higher reverse recovery peak. Nevertheless, current source driving still provides lower losses than standard Rg driving.

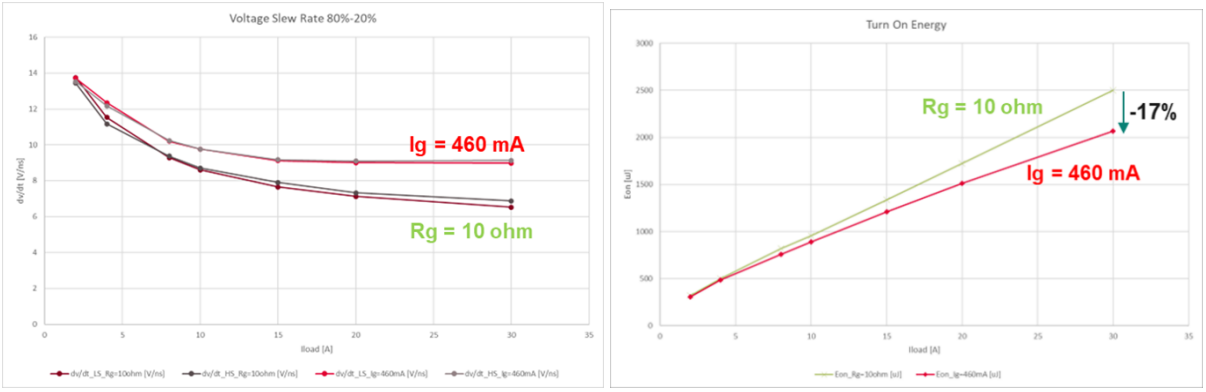


Figure 9 Characterization result of Advance GD with IGBT power switches, (a) dV/dt controllability is less with respect to SiC MOSFET, (b) but comparing with Rg driving, it results in an Eon decreases.

A second optimize demonstrator is developed able to generate a constant level output current, reported in figure 10. It can be plugged in a double pulse setup board. Receiving at the input the output of a standard GD IC, it generates a constant output current, which level can be set by selecting the proper resistor on the board, though a jumper.

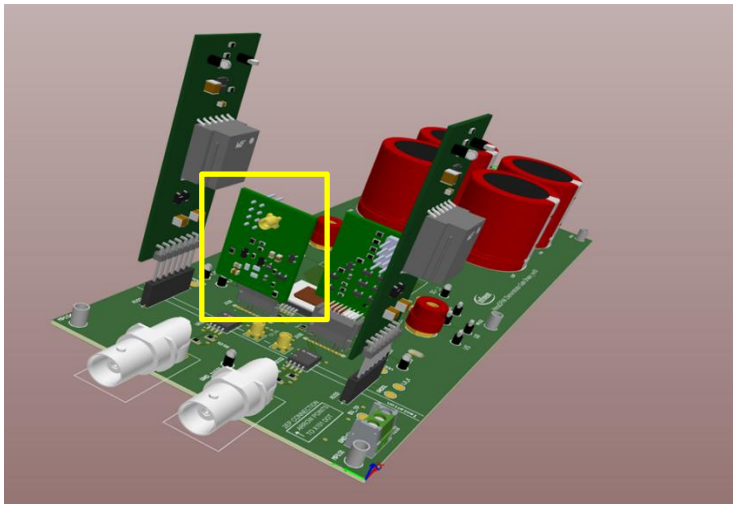


Figure 10: Compact and optimize version of constant current GD

For the multi-level gate-current method, the waveform generated by the demonstrator is shown in Figure 11. The parameters t_delay, t_pulse, and I_gk can be adjusted to tailor the switching behaviors of the power device.

The optimal switching pattern has been obtained, in simulation, with a genetic optimization algorithm based on differential evolution. Figure 12 shows the results of the optimization procedure.

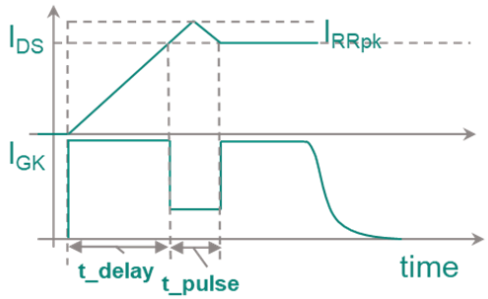


Figure 11 Multilevel output current waveform. It is possible to control t_delay, t_pulse and I_{GK} to optimize the switching performance.

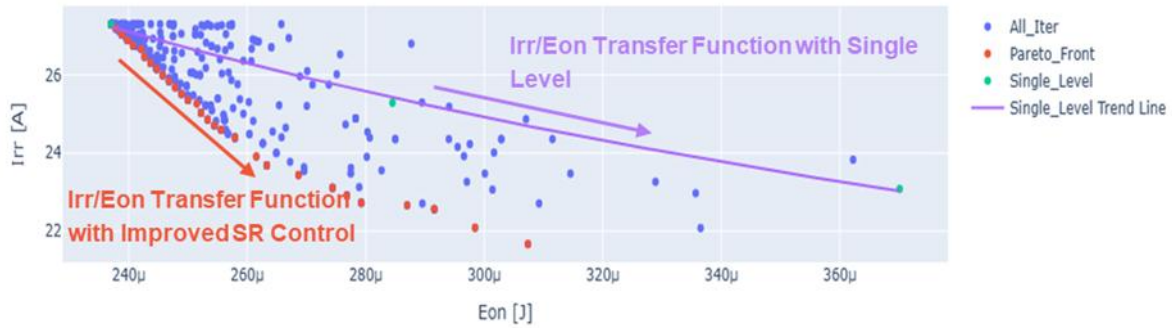


Figure 12 Multi level current source, optimization engines results.

The demonstrator was evaluated in a laboratory setting with conventional benchtop instrumentation. Due to its fully analog architecture, operation did not require a Digital Signal Processor (DSP) or any

auxiliary digital control. This method is tested with SiC power switches and results are shown in figure 13.

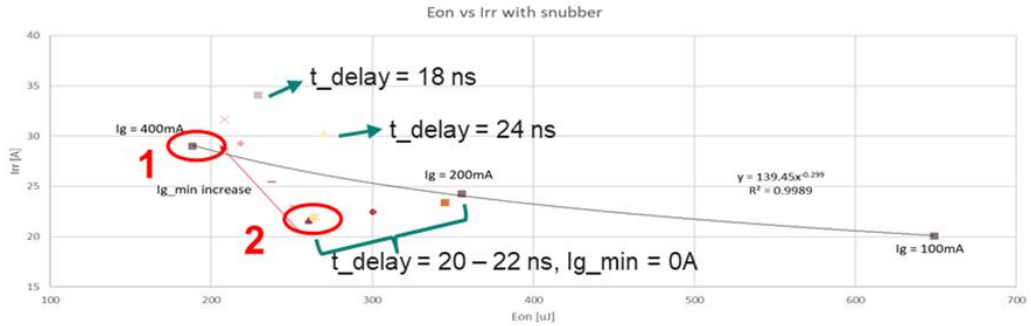
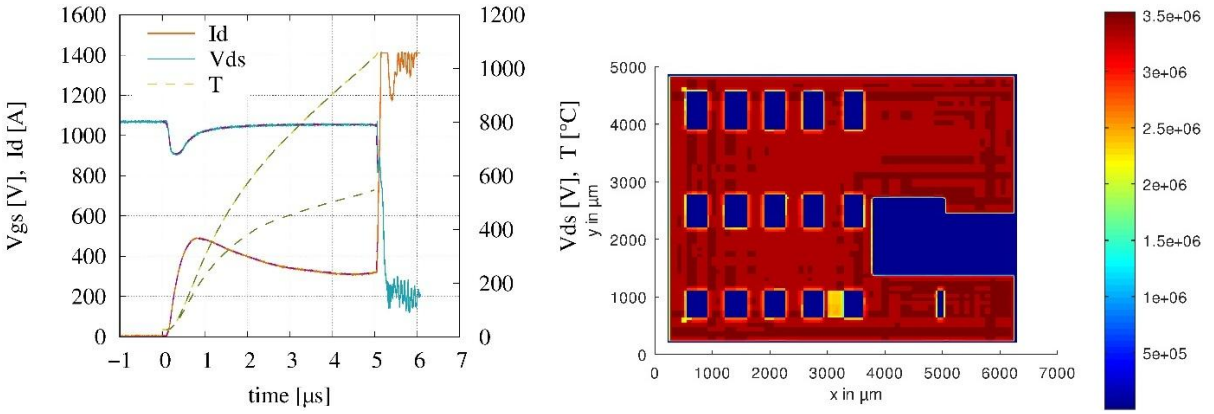


Figure 13 I_{RR} and E_{ON} Graph with multi-level source driving results.

In this case, it is possible to observe that the multi-level current source driving enables a new transfer function between the reverse recovery peak (directly linked to EMI) and the Eon. Hence, this new driving method allows us to reduce both EMI and switching losses. Self-powered sensing does not exist commercially neither as state-of-the-art R&D for train applications nor for other applications that could easily be transferred to Alstom case.

In **WG3**, **TUDO** working together with **KTH**, has developed a physics-based model of a SiC-MOSFET, utilizing an extensive number of short-circuit-tests at different operating points and temperatures. The model has been developed by utilizing a finite-volume-method, which accounts for temperature dependent thermal-resistance and thermal-capacity, thus being able to account for inhomogeneous current densities, e.g. due to operation below the zero-temperature-coefficient-point or localized cooling due to bond contacts. By utilizing the model, the SOA-limits are well-defined and provide the dynamic boundaries of operation, which can be used as a basis to optimize advanced gate-patterns.



In WG4, KTH has developed and experimentally validated an advanced gate driver concept for wide-bandgap SiC MOSFETs, enabling autonomous soft-switching operation suitable for high-voltage traction inverters. The work focuses on **Autonomous Gate Drivers (AGDs)** that perform all switching decisions locally at the gate-driver level without requiring external digital control, directly supporting the objectives of WP2.3 in intelligent sensing and control.

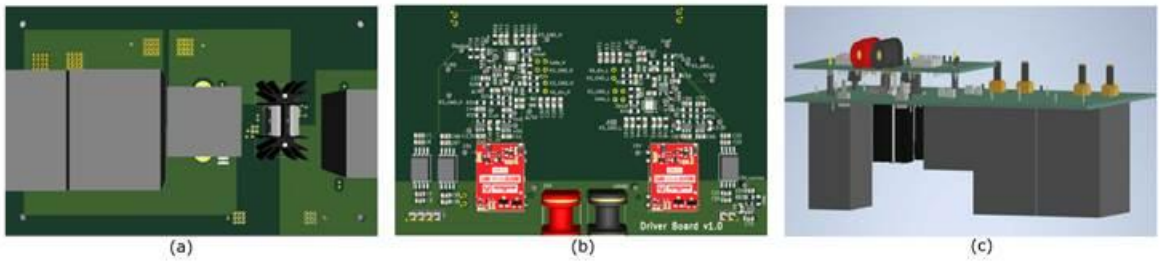


Fig. 4. PCB layout of the AGD-based soft-switched buck converter: (a) Power board, (b) Controller board, and (c) Integrated assembly of the power and controller boards.

The designed converter operates at a 400 V DC-link voltage and achieves **Zero-Voltage Switching (ZVS)** during both turn-on and turn-off transitions through **Triangular Current Mode (TCM)** operation. The key feature of the developed AGD is its ability to sense both voltage and current directly at the device level and to act upon them in real time. The **drain-source voltage (Vds)** is monitored to ensure turn-on at zero voltage, while the **on-state resistance (Rds(on))** of the MOSFET is used as an internal current-sensing element for determining the peak current and initiating turn-off.

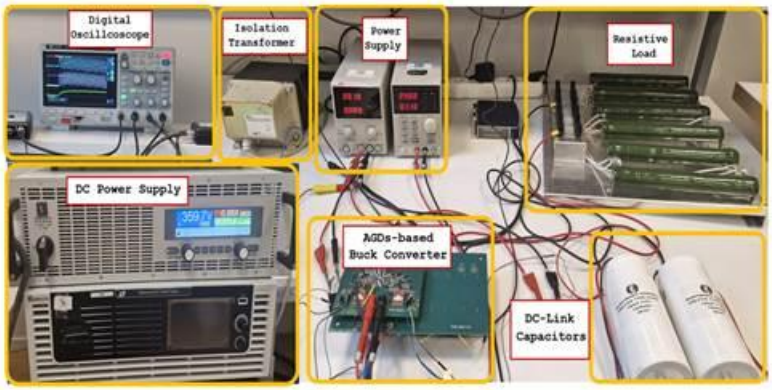


Figure 4.3: Setup for experimental validation of the AGD-enabled soft-switching buck converter

All sensing and control are performed by analog circuitry integrated within the gate driver, including high-speed comparators, an RS latch, startup circuitry, and a galvanically isolated current reference. This architecture eliminates external feedback loops and high-bandwidth signal paths, allowing for extremely fast and reliable switching control.

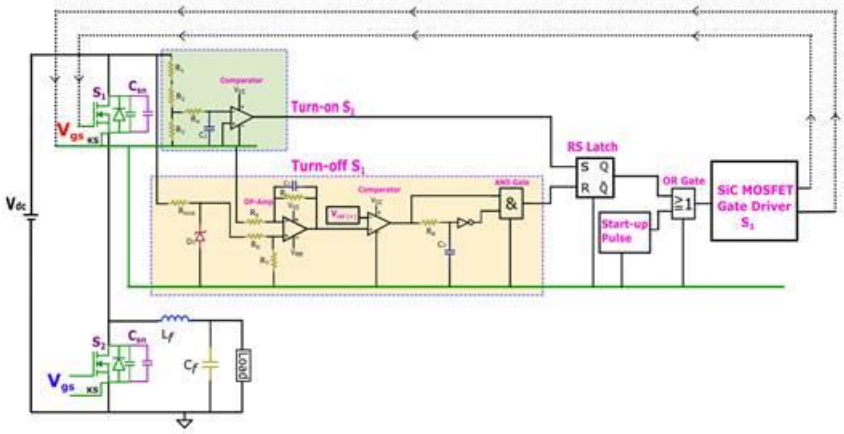


Figure 4.1: Functional diagram of the AGD circuit implemented for the high-side SiC MOSFET in a ZVS buck converter.

A fully functional **soft-switched buck converter prototype** based on the AGD concept was designed and tested to verify the concept. Experimental validation confirmed:

- Stable ZVS transitions at 400 V DC-link voltage,
- Peak-to-peak inductor current of 35 A ensuring operation within TCM,
- Switching transition times in the range of 130–170 ns depending on load current,
- Suppression of voltage overshoot and reduced switching energy loss due to optimized snubber capacitance.

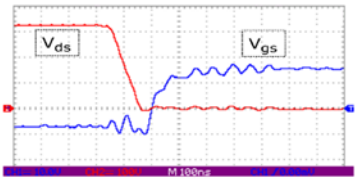


Figure 4.8: Measured waveforms illustrating turn-on ZVS: the switch is turned on as the drain-to-source voltage (V_{ds}) becomes slightly negative and the gate-to-source voltage (V_{gs}) rises. Scale: CH1 = 10 V/div, CH2 = 100 V/div.

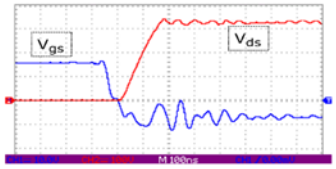


Figure 4.9: Measured waveforms demonstrating turn-off ZVS: the gate-to-source voltage (V_{gs}) drops to a negative value before the drain-to-source voltage (V_{ds}) begins to rise. The slope of V_{ds} is influenced by the snubber capacitance. Scale: CH1 = 10 V/div, CH2 = 100 V/div.

The results demonstrate that the AGD enables high-efficiency, low-EMI operation while simplifying converter control. Future work will focus on implementing temperature-compensated current sensing, refining filter design to reduce ripple, and extending the AGD concept to multi-phase inverter systems for traction and industrial applications.

In WG5, RISE is working with **ALSTOM** in **UC1.1** to develop **self-powered sensing system** based on energy harvesting solutions such that in-field measurements can be performed. This real data is needed to improve Alstom's simulation model of power electronics in the train, the prototype for energy harvesting system contains energy harvester itself, measurement electronics, microcontroller, energy storage, sensors and low-power wireless communications. For these developments, some commercial components are used for shorting the development time (electronics, BLE, Wi-Fi). The innovation is on the i) design of harvester itself, ii) design for measurement electronics for extremely low-power consumption, iii) design of the whole harvesting system, and iv) development of the lab characterisation set-up for thermal harvesting at RISE for obtaining precise and stable temperature gradient as low as 0,25^{o}C.

Two energy harvesting technologies were developed and successfully tested at Alstom lab:

1) **Thermoelectric harvesting** using the temperature gradient – Two generation prototypes were developed and tested at Alstom lab showing very good results for cold start of the system at circa 6°C temperature gradient.
2) **Inductive harvester** using the magnetic field generated by the high electrical current
   a) Two generation prototypes were developed and tested at Alstom lab showing excellent results. There is enough harvested energy to power BLE communication up to 15-20m indoor but also for other type (Wi-Fi, 4g) and to power conventional sensors (e.g. temperature, humidity).

b) Few generations of electronics modules to i) allow not only BLE but also Wi-Fi; ii) protection electronics against large amounts of energy for the energy storage (e.g. rechargeable battery), iii) compact layout; iv) easier flashing of processor via USB.

In WG6, FPG and **HEPO** worked on concepts and interfaces for analyzing state and health of battery, grid and load. The results show a significant difference in SOH after charging either with CC/CV or pulsed charging. For analyzing grid and load characteristics, neural networks have been created which work inside the used controller platform for the digital energy flow control.
The test setup with charger, battery and SOH measurement is shown in Figure 34:

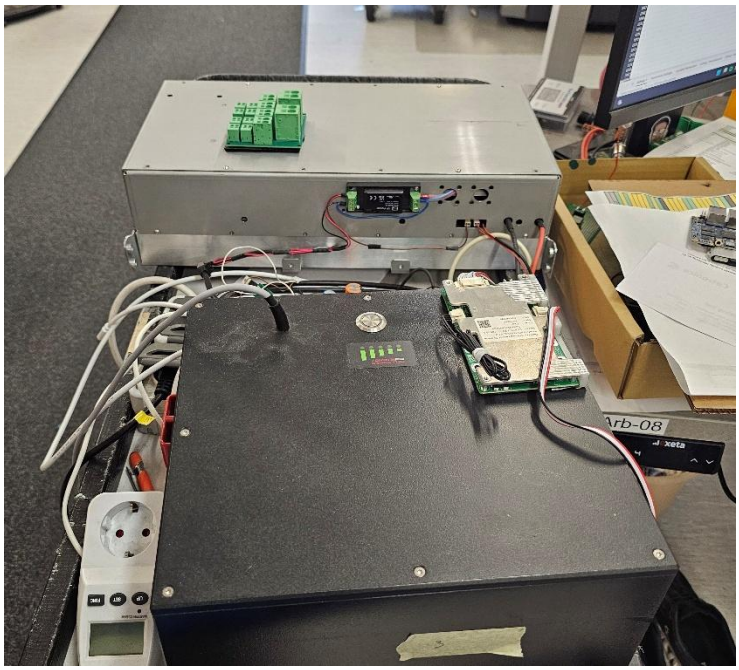


FIGURE 34

Adaptive PWM control - FPG

In **adaptive PWM control** task **FPG** performed SPICE analysis for a PFC operation coupled with a control method and auxiliary circuit for decreasing the overall losses. The lab testing showed a loss reduction by 50% for the main switches, which are now switching ZVS instead of hard-switching, however additional unexpected high losses occur in the auxiliary circuit which lower the loss reduction again. Finally, some optimization measured could be defined in order to compensate this effect to a certain level. Table 1 shows the simulated result of the tested operating point for switching loss reduction.

Component	Losses without AUX circuit	Losses with AUX circuit	Change
High Side switch	2,21 W	0,91 W	-59%
Low Side switch	4,83 W	2,31 W	-52%

TABLE 1

Multirate – XC

XC is working on the **Multirate** task. For the multirate task a control scheme with a fast inner loop (>= 100kHz) for current control and a slower voltage control loop is implemented. The current control loop is processed on an FPGA to achieve short computation times, while the voltage loop runs on a microcontroller. A demonstrator controller board that includes all the hardware needed to sense the system state is developed. On that board, multiple measuring methods were implemented. The microcontroller is placed on a second board which is mounted on the baseboard. The microcontroller is also able to measure the physical values necessary to perform the slow control scheme. Design is realized to be as flexible as possible to compare the different methods of measurement with respect to their suitability towards high bandwidth control applications. Goal of moving the fast control loop on the FPGA is to match the trend towards high switching frequencies without running into limitations imposed by the computation time of the microcontroller.

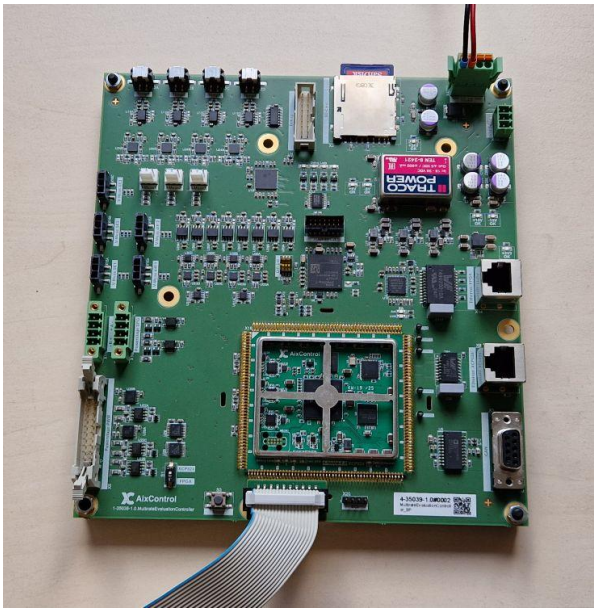


FIGURE 4: BASEBOARD WITH MOUNTED MICROCONTROLLER BOARD

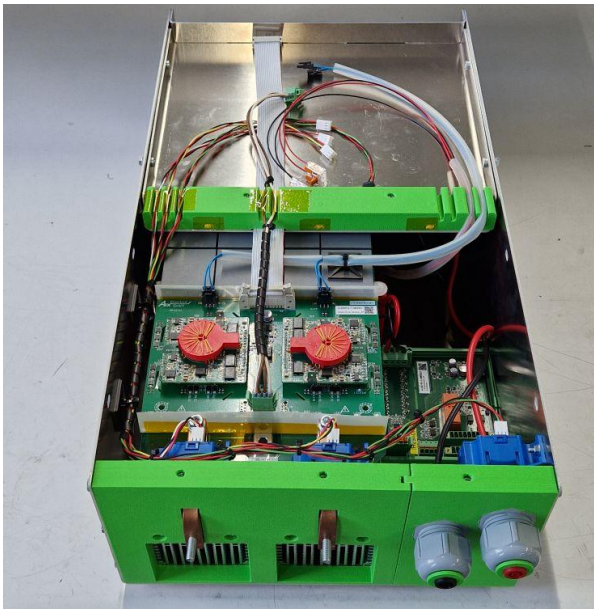


FIGURE 5: INVERTER STAGE FOR TESTING OF HIGH BANDWIDTH CONTROL

The concept of the high bandwidth, multirated control was elevated to an implemented design featuring both the fast loop on the FPGA as well as the slower loop on the microcontroller. Simultaneously, a baseboard holding the FPGA and a mountable microcontroller board were realized. The baseboard is equipped with a variety of different measurement schemes to test their suitability for the control task at hand. Existing hardware was adapted to provide an inverter stage fit for testing with the desired high control frequency.

Transient thermal impedance -TUDD

The individual task of determining the transient thermal impedance of the module was successfully completed by TUDD. Temperature measurements were conducted using both an in-situ sensor and the NTC thermistor embedded within the IGBT module under varying load currents. The collected data were subsequently analyzed.

In Figure 15, the measured in-situ temperature $\vartheta_{jonchip}$, the temperature calculated via the V_{ce}-method ϑ_{Vce} and the NTC temperature ϑ_{ref} are presented for a load current of 400 A. A comparison between the in-situ measurement and the V_{ce}-derived temperatures reveals excellent agreement in their dynamic behavior. A key advantage of the in-situ measurement is its ability to provide temperature data during the conduction phase, when the load current flows through the IGBT.

The Figure illustrates also the transient thermal impedance, derived from the temperature difference between the in-situ sensor and the NTC.

The results demonstrate the feasibility of determining transient thermal impedance using the recorded measurements. Notably, a slight overshoot in the calculated transient thermal impedance is observed within the time range of approximately 2 s to 10 s. This phenomenon is attributed to the delayed response characteristic of the NTC temperature measurement.

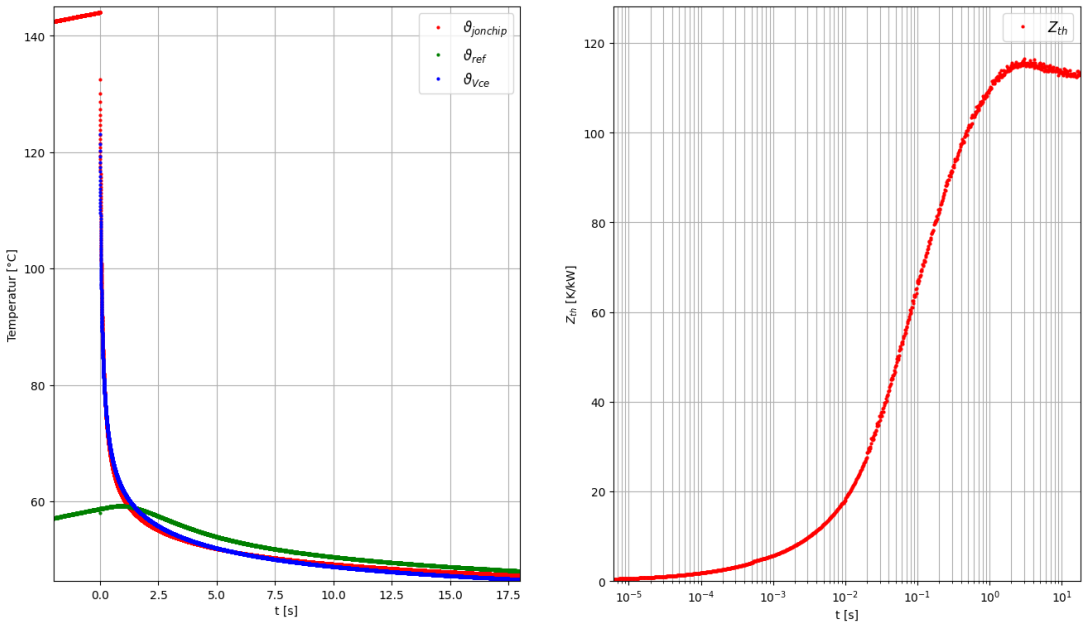


FIGURE 15: MEASURED IN-SITU TEMPERATURE, TEMPERATURE CALCULATED USING THE V_{CE}-METHOD, AND NTC TEMPERATURE AT A LOAD CURRENT OF 400 A

Monolithically integrated SiC Sensor - TUDE

The DOE for a comprehensive study of process parameter effects on Inductively coupled plasma reactive ion etching (ICP-RIE) process optimization was conducted. The optimization goal for etch rate, mask selectivity, and defect suppression was taken into consideration for the optimization.

The RIE process setup is based on Adixen AMS 110 and Plasma Pro 100 Estrelas. Single parameter sweeps for substrate bias power, pressure, substrate temperature, and ICP source power were conducted to study the parameter effect. As shown in Figure 16, a correlated effect between pressure and substrate bias power was observed. Both the pressure and the substrate bias power can significantly affect the physical bombardment of ions on the sample. Since the ion bombardment strength is critical to initiate the etching, while undermining the mask selectivity, a trade-off decision needs to be made for etch rate, selectivity, and micro-masking effect suppression.

High bias power, low pressure is the superior setting, though at the cost of losing selectivity.

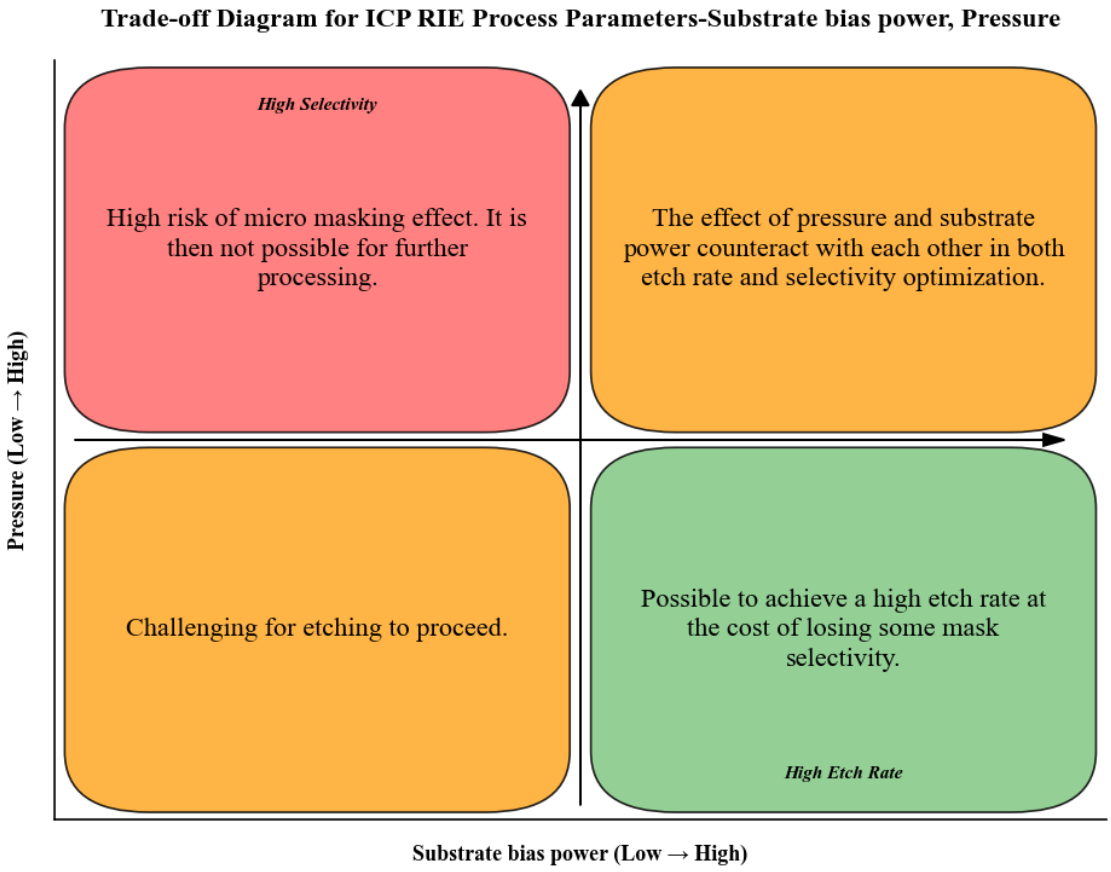


Figure 16: Trade-off Diagram for ICP RIE Process Parameters-Substrate bias power, Pressure

When applying high pressure and low substrate bias power, the risk of grass formation on the sample is significantly high. Figure 17 is an example of a massive grass formation (micro masking effect) when high pressure is applied. Only 2.59 um were etched in 10 minutes. The massive micro pillars on the etched surface make further processing impossible.

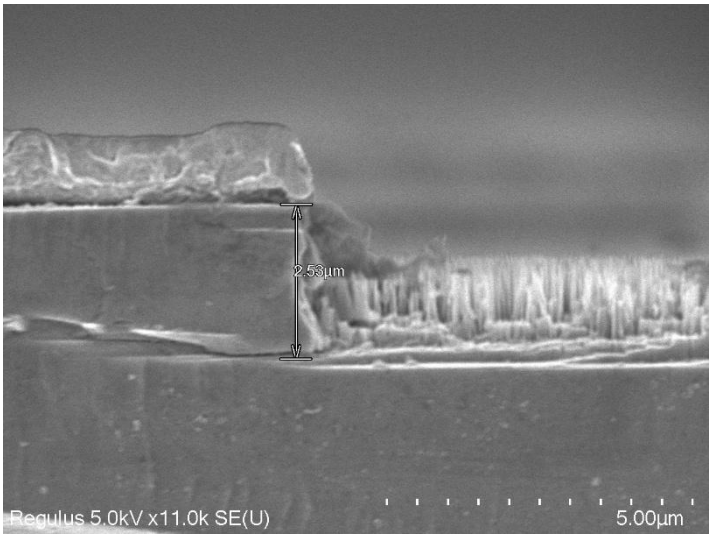


Figure 17: Micro masking effect observed on samples etched with high pressure

Parameter sweep of substrate temperature, from cryogenic conditions to room temperature (RT), and the sweep of ICP source power were also conducted. As shown in Figure 18, in the temperature range between cryogenic conditions and RT, the etch rate on SiC material dominates the selectivity, which is the reason why higher etch rate and selectivity were achieved in the same quadrant.

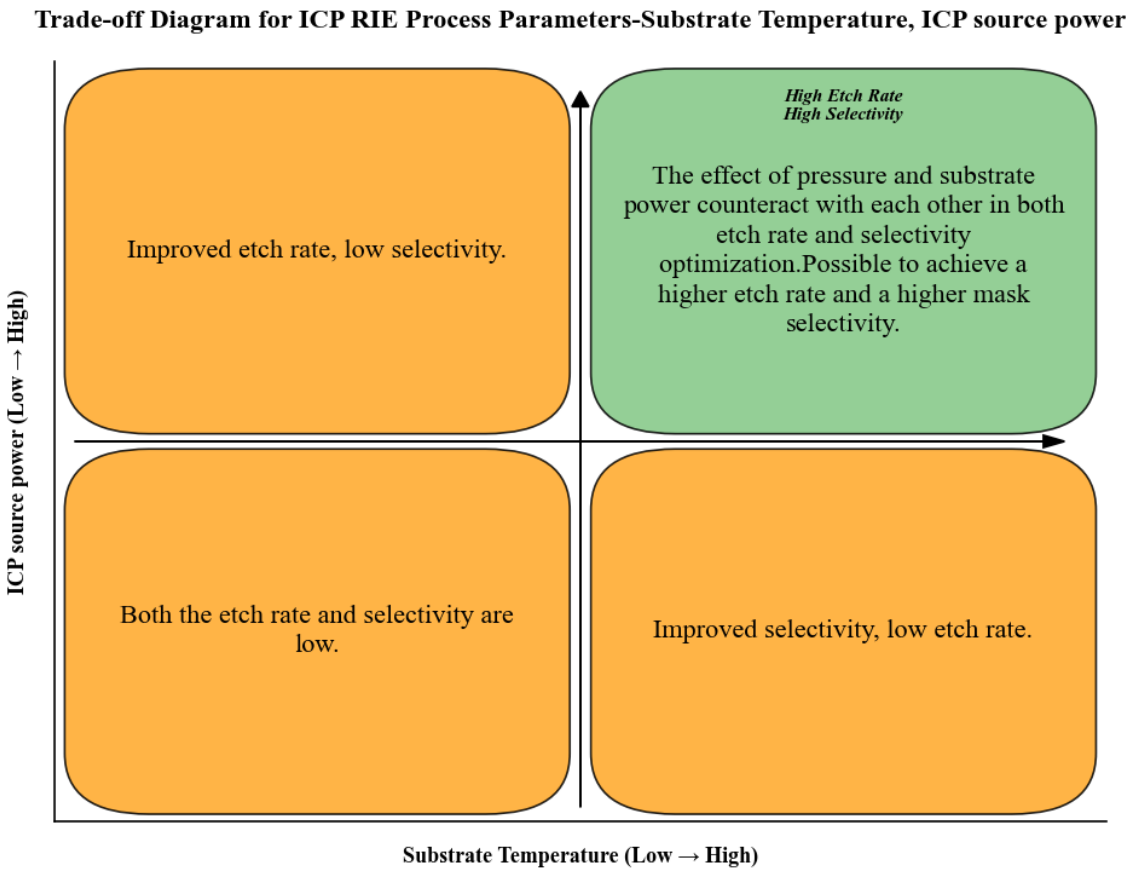


Figure 18: Trade-off Diagram for ICP RIE Process Parameters-Substrate Temperature, ICP source power

In addition, the etch rate can differ between different design patterns. Figure 19 presents the profiling of the etch depth difference between two inverted patterns. It is observed that even with the same image design, if the patterns are inverted, the etch depth can differ significantly. This is due to the area of surface exposed to etch gases, which indicates a different consumption rate of etchants. So, for accurate sensor fabrication, the sensor structure pattern geometry uniformity should also be taken into account.

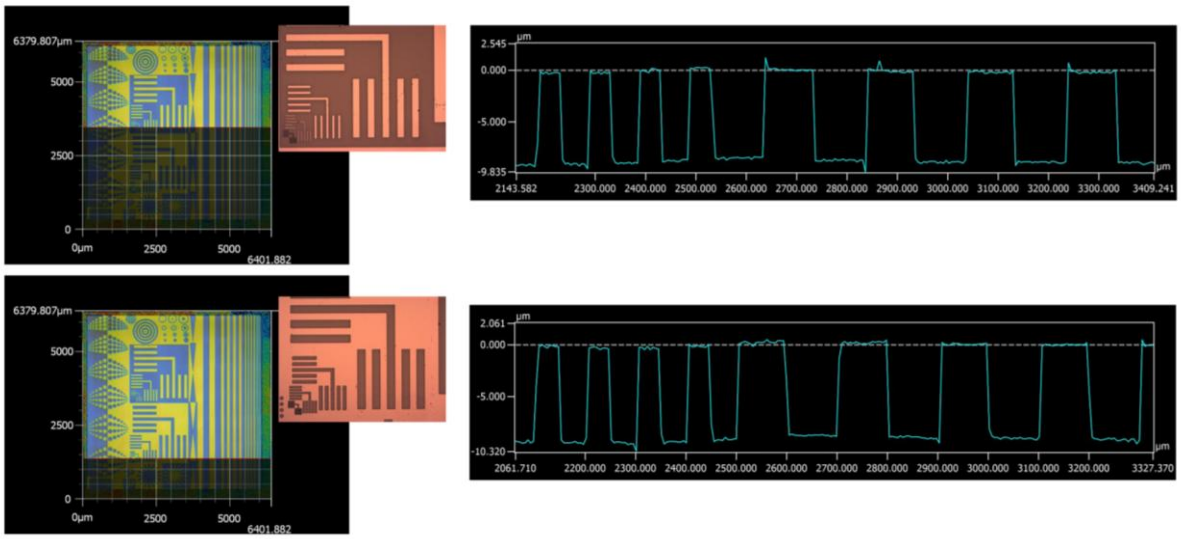


Figure 19: Surface profiling of two inverted patterns after ICP RIE process

2.3 Conclusions

In light of the results obtained during Reporting Period 3, we have updated the status of the KPIs and measures of success defined at the beginning of the PowerizeD project.
WP2.3 achieved the planned results in the field of Intelligent Sensing and Control.

KPIs and measure of success	**Status at the time of writing**
Adjustment of the on-state forward voltage by 20% based on the nominal on-state voltage	COMPLETED Measurements confirmed that by varying Vge in the range of 11 V to 19 V, the Vce of the two investigated modules can be altered by approximately 24 % and 30 % compared to their nominal values at rated current.
Online control algorithm, which adjusts the dv/dt without previous calibration	COMPLETED Concepts for adjusting the on-state forward voltage and online dv/dt control were developed, prototypes were built, and initial measurements for dv/dt control were conducted. TUDD worked on IGBT in motor drive application, demonstrating a dV/dt controllability from 3.8 to 10.4 kV/µs. EDI and IFI worked on SiC MOSFET implementation.
Decrease switching power losses by 50% in a target application allowing the optimization of switching speed	COMPLETED In TASK PWM: Met KPI (Loss reduction by 50% in the switches)
Extend SW functionality to analyze grid, load, battery and PV characteristics	COMPLETED In WG6: the battery SOH detection and influence of charging characteristics showed 3% difference in SOH for the tested charging cycles.

Two WBG sensor solutions available within the project	COMPLETED TUDE completed an optimized Inductively coupled plasma (ICP) reactive ion etching process (RIE) development for SiC based sensor fabrication. A standard for process tuning has been established. TUDO has developed a digital twin for SiC. By utilizing the model, the SOA-limits are well-defined and provide the dynamic boundaries of operation, which can be used as a basis to optimize advanced gate-patterns By developing an inductive energy harvesting system (RISE) for the power electronics module from Alstom, it is possible to send sensor data (temp, humidity) by BLE from inside the metal casing by using the harvested energy from the high current values. The sensors system's battery lifetime is extended indefinitely by using this inductive harvester.
Sensor accuracy +35%	COMPLETED TUDE completed the ICP-RIE process DOE test for accurate sensor structure realization. Detrimental factors impeding the accuracy of sensor fabrication such as micro-masking effect have been suppressed. It can be concluded that a significant (more than 99%) defect suppression on the surface is achieved. Definitely, the accuracy of overall SiC sensor fabrication in terms of trench structure realization is improved by more than 35%.

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